Subject Name:-ANALOG and DIGITAL ELECTRONICS

Teacher Name :- Mr. Prasanta Kumar Parida

Subject Code:-

Semester- 3rd

Branch-EEE

Course-B.Tech

SYLLABUS CONTENTS

MODULE-I(9 HOURS)

- Biasing of BJT: Fixed bias circuit, Self-bias circuit, Feedback bias circuit, Bias Stabilization. Transistor at Low Frequencies: Transistor Hybrid Model, h- parameters, Analysis of the transistor amplifier using h-parameter. Emitter Follower, Miller's theorem and its dual, cascading transistor amplifiers, Simplified CE and CC configurations. Transistor at high frequency: Hybrid-pi CE Transistor Model.

MODULE-II (6 HOURS)

- Biasing the JFET: FET in fixed bias, self-bias and feedback bias configurations. FET small signal modelling. Frequency response of an amplifier, Bode plot, Band pass of cascaded stages, RC-Coupled amplifier and its low frequency response. Classification of amplifier, Feedback concept, Transfer gain, Negative feedback, Input-output resistance, Method of analysis of a feedback amplifier, Voltage series feedback, Current series feedback, Voltage shunt feedback, Current shunt feedback.

MODULE-III (9 HOURS)

- The basic operational amplifier (OPAMP), Off-set error voltages and currents, temperature drift of input offset voltage and current, measurement of OPAMP parameters and its frequency response. Class –A large signal amplifier, higher order harmonic generation, Transformer coupled audio amplifier, push-pull amplifier.

Digital circuits: Digital (Binary) operation of a system, OR gate, AND gate, NOT or inverter circuit, De Morgan's laws, NAND and NOR DTL gates, HTL gate, TTL gate, RTL and DCTL.

- **MODULE-IV (6 HOURS)**

Binary codes: BCD codes, gray codes, ASCII Character Code, Boolean Algebra & Logic gates: Axiomatic definition of Boolean algebra. Property of Boolean algebra, Boolean functions, Canonical & standard form; min terms & max terms, standard forms; Digital Logic Gates, Multiple inputs. Gate level Minimization: The Map Method, K Map up to five variables, Product of Sum simplification, Sum of Product simplification, Don't care conditions.

MODULE-V (9 HOURS)

- Combinational digital systems: Standard gate assembles, Binary adder, arithmetic functions, Decoder/De-multiplexer, Data selector/Multiplexer, Encoder. Sequential digital systems: A 1-bit memory, Flip-flops, shift registers, Ripple (Asynchronous) counters, Synchronous counters, Application of counters.

TEXT BOOKS

[1]. Milliman. J, Halkias. C and Parikh. C.D., “Integrated Electronics”, Tata Mc. Graw Hills 2nd Ed. 2010.

[2]. R.L Boylestad and L. Nashelsky, “Electronic Devices & Circuit Theory:, Pearson Education.

[3]. M. Morris Mano, “Digital Design”, PHI Publishers.

REFERENCE BOOKS

[1]. Mohammad Rashid, “Electronic Devices and Circuits”, Cengage Learning Publishers.

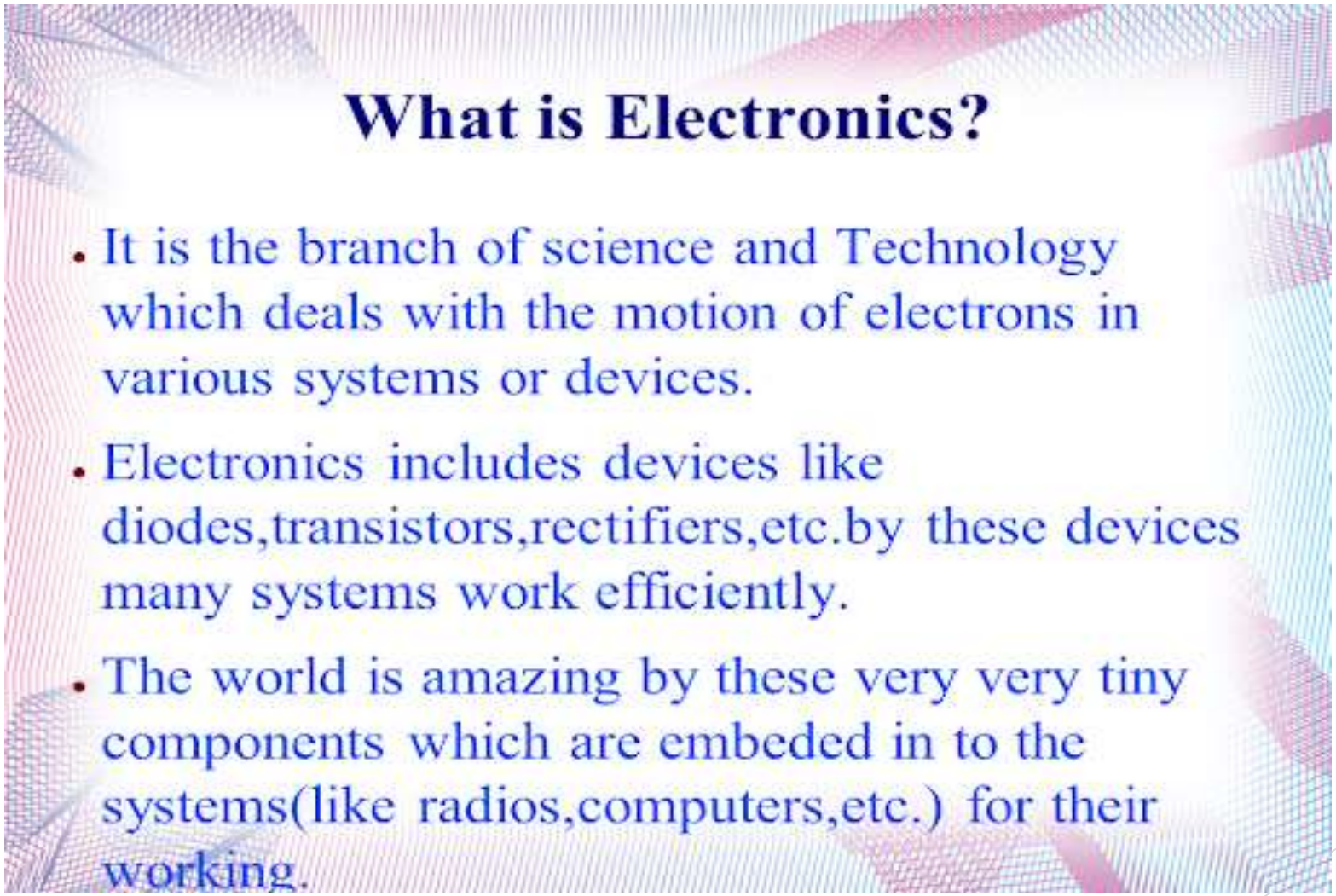
[2]. Sergio Fransco, “Design with Operational Amplifiers& Analog Integrated Circuits”, TMH Publishers.

[3]. Charles H.Roth, “Fundamentals of Logic Design”, Cengage Learning Publishers

Contents

- Introduction to **ANALOG AND DIGITAL ELECTRONICS CIRCUITS.**
- **Fundamentals of BJT**

Introduction:



- Analog Electronics are electronics system with a continuously varying signal.
- Digital Electronics are electronics that handle digital signal.

Factors	Analog	Digital
Waves	Denoted by Sine waves	Denoted by Square waves
Signal	Continuous signal representing physical measurements	Discrete signal representing discrete time signals generated by digital modulation
Data Transmission	Subject to deterioration by noise	Noise-immune without deterioration
Bandwidth	Consumes less bandwidth	Consumes more bandwidth
Memory	Stored in the form of wave signal	Stored in the form of binary bit
Power	Draws large power	Draws negligible power
Impedance	Low impedance	High order of 100 megaohm
Errors	Analog instruments have considerable observational errors	Digital instruments are free from observational errors

Fundamentals of BJT:

- Few most important applications of transistor are: as an amplifier, as an oscillator and as a switch.
- BJT is bipolar because both holes (+) and electrons (-) will take part in the current flow through the device

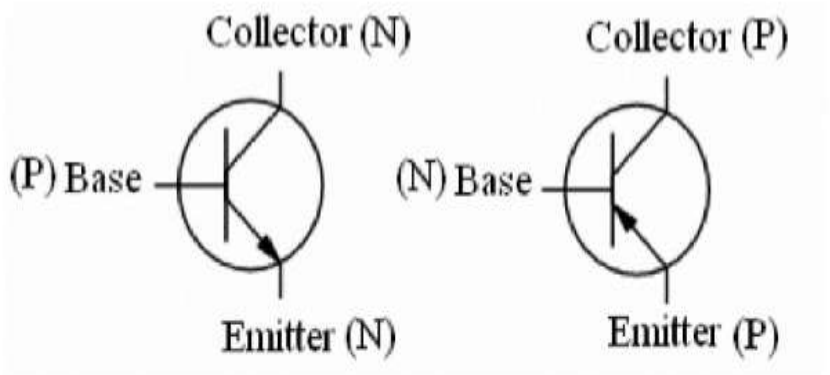
– N-type regions contains free electrons (negative carriers)

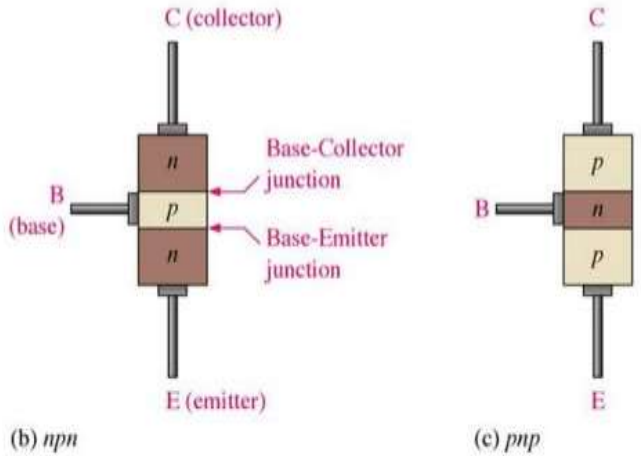
– P-type regions contains free holes (positive carriers)

- From the physical structure, BJTs can be divided into two groups: ***npn*** and ***pnp*** transistors.

Transistor Structure

- In diodes there is one p-n junction.
- In **Bipolar junction transistors (BJT)**, there are three layers and two p-n junctions.





Note: Arrow Direction from P to N (Like Diode)

BASIC OPERATION OF TRANSISTOR

- There are three mode of operations:

Bias Mode	***E-B Junction***	***C-B Junction***
Saturation	Forward	Forward
Active	**Forward**	**Reverse**
Inverted active	Reverse	Forward
Cutoff	Reverse	Reverse

- If transistor is operating active mode, it can be used as amplifier.
- The transistor can be used as logical switch if it operates in cut-off and saturation mode.

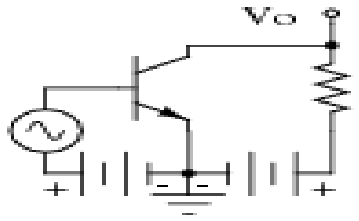
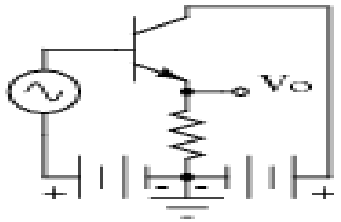
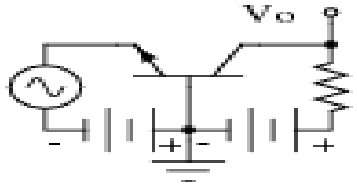
Transistor Configuration:

- Depending upon the terminals which are used as a common terminal to the input and output terminals, the transistors can be connected in the following three different configuration.

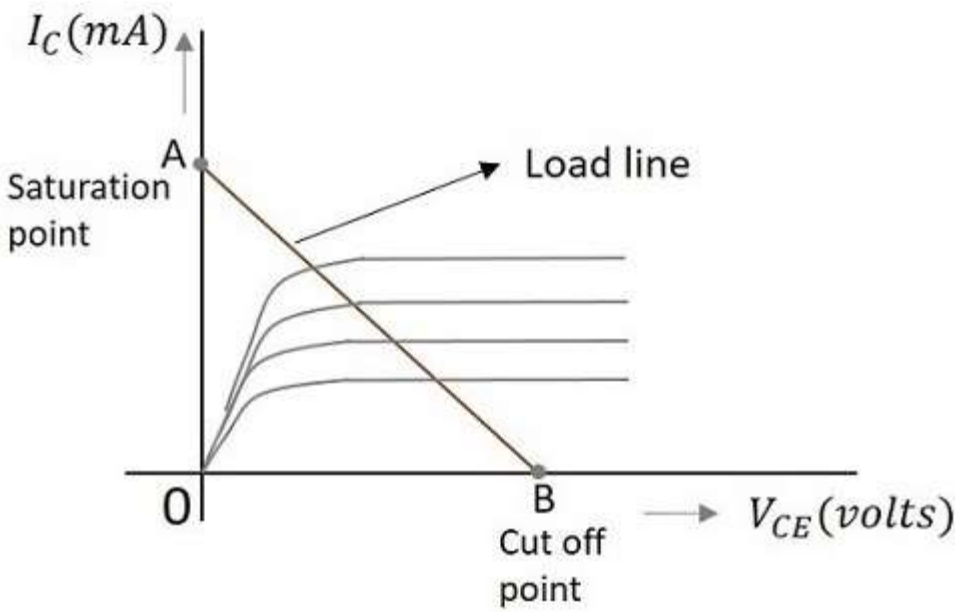
1. common base configuration

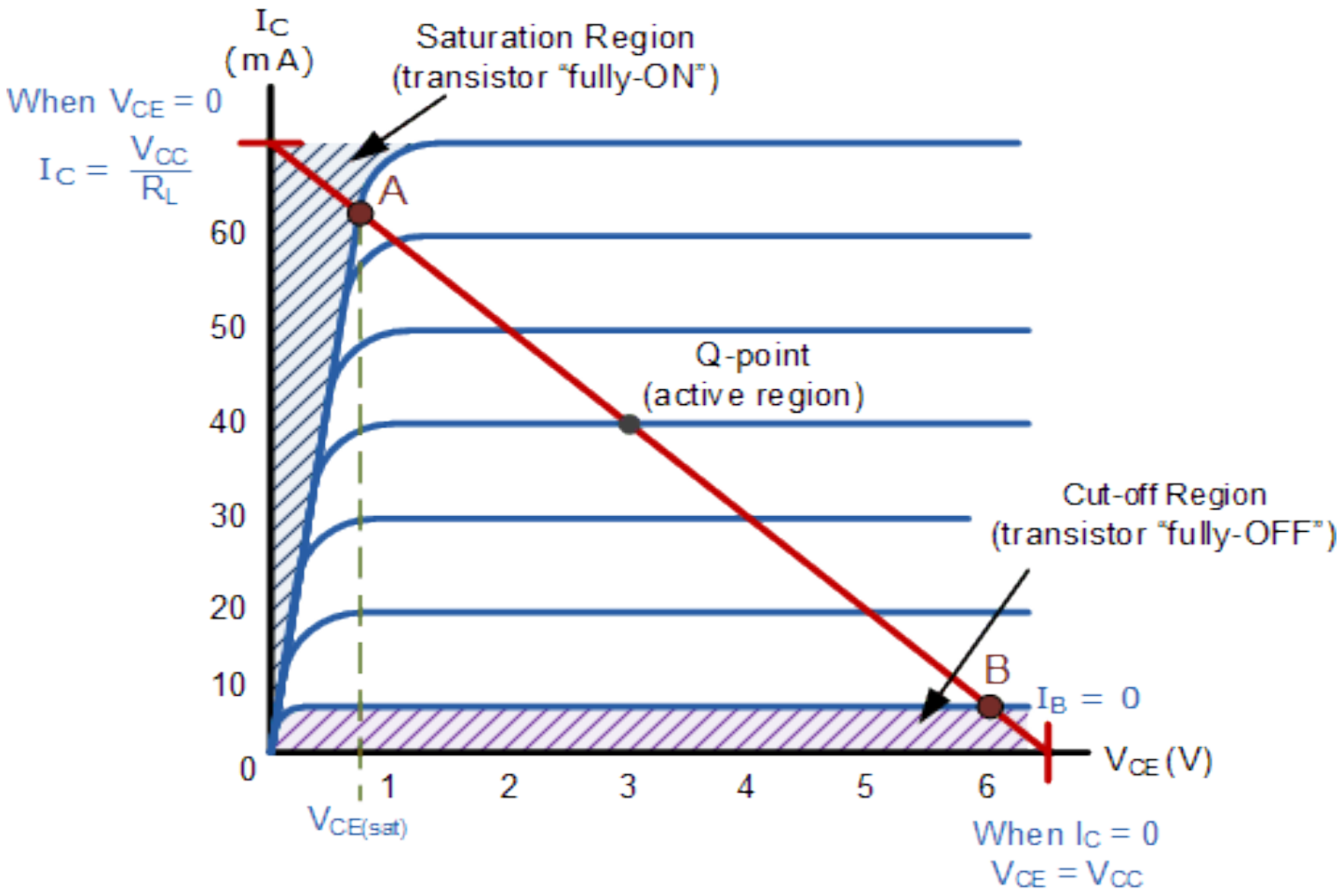
2. common emitter configuration

3. common collector configuration

Basic circuit	Common emitter	Common collector	Common base
			
Voltage gain	high	less than unity	high, same as CE
Current gain	high	high	less than unity
Power gain	high	moderate	moderate
Phase inversion	yes	no	no
Input impedance	moderate ≃ 1 k	highest ≃ 300 k	low ≃ 50 Ω
Output impedance	moderate ≃ 50 k	low ≃ 300 Ω	highest ≃ 1 Meg

Load Line and Q-point:




I_C (mA)
Saturation Region
(transistor "fully-ON")
When $V_{CE} = 0$
$I_C = \frac{V_{CC}}{R_L}$
A
60
50
Q-point
(active region)
40
30
Cut-off Region
(transistor "fully-OFF")
20
B
10
$I_B = 0$
0
1
2
3
4
5
6
V_{CE} (V)
$V_{CE(sat)}$
When $I_C = 0$
$V_{CE} = V_{CC}$

- Load Line:

When a value for the maximum possible collector current is considered, that point will be present on the Y-axis, which is nothing but the **Saturation point**.
As well, when a value for the maximum possible collector emitter voltage is considered, that point will be present on the X-axis, which is the **Cutoff point**.
When a line is drawn joining these two points, such a line can be called as **Load line**.

This is called so as it symbolizes the output at the load. This line, when drawn over the output characteristic curve, makes contact at a point called as **Operating point** or **quiescent point** or simply **Q-point**.

- DC Load Line

When the transistor is given the bias and no signal is applied at its input, the load line drawn under such conditions, can be understood as **DC** condition. Here there will be no amplification as the **signal is absent.**

Q-Point (Static Operation Point)

- When a line is drawn joining the saturation and cut off points, such a line can be called as **Load line**. This line, when drawn over the output characteristic curve, makes contact at a point called as **Operating point**.
- This operating point is also called as **quiescent point** or simply **Q-point**. There can be many such intersecting points, but the Q-point is selected in such a way that irrespective of AC signal swing, the transistor remains in the active region.
- The operating point should not get disturbed as it should remain stable to achieve faithful amplification. Hence the quiescent point or Q-point is the value where the **Faithful Amplification** is achieved.

Applications of BJT

- Discrete-circuit design.
- Analog circuits.
- High frequency application such as radio frequency analog circuit.
- Digital circuits.
- Bi-CMOS (Bipolar+CMOS) circuits that combines the advantages of MOSFET and bipolar transistors.
  - MOSFET: high-input impedance and low-power.
  - Bipolar transistors: high-frequency-operation and high-current-driving capabilities.

Thank you.

Contents of this class

- What is biasing circuit?
- Purpose of the DC biasing circuit
- Different Biasing circuits
- Fixed bias (base bias)
- Emitter bias

- The analysis or design of any electronic amplifier therefore has two components: The dc portion and The ac portion

During the design stage, the choice of parameters for the required dc levels will affect the ac response.

- **What is biasing circuit?**

This process of selecting proper dc supply voltages and resistance for obtaining desired operating point or Q point is called as biasing and the ckt used for transistor biasing is called as biasing ckt.

- **Purpose of the DC biasing circuit**

• To turn the device “ON”

• To place it in operation in the region of its characteristic where the device operates most linearly, i.e. to set up the initial dc values of *IB*, *IC*, and *VCE*

- There are four conditions to be met by a transistor so that it acts as a faithful amplification:

1)Emitter base junction must be forward biased (VBE=0.7Vfor Si, 0.2V for Ge) and collector base junction must be reverse biased for all levels of i/p signal.

2) Vce voltage should not fall below VCE (sat) (0.3V for Si, 0.1V for Ge) for any part of the i/p signal. For VCE less than VCE (sat) the collector base junction is not probably reverse biased.

3) The value of the signal Ic when no signal is applied should be at least equal to the max. collector current due to signal alone.

4) Max. rating of the transistor Ic(max), VCE (max) and PD(max) should not be exceeded at any value of i/p signal.

- Even though the Q point is fixed properly, it is very important to ensure that the operating point remains stable where it is originally fixed. If the Q point shifted, the output voltage and current get clipped, thereby o/p signal is distorted.

- In practice, the Q-point tends to shift its position due to any or all of the following three main factors.

1) Reverse saturation current, Ico, which doubles for every 10oC raise in temperature

2) Base emitter Voltage ,VBE, which decreases by 2.5 mV per oC

3) Transistor current gain, hFE or ß which increases with temperature.

Important basic relationship

- $V_{BE} = 0.7V$
- $I_E = (\beta + 1)\, I_B \cong I_C$
- $I_C = \beta\, I_B$

- **Different Biasing circuits:**

- Fixed bias (base bias)
- Emitter bias
- Voltage divider bias(self bias)
- DC bias with voltage feedback

1)Fixed bias (base bias)

- The simplest transistor dc bias configuration.
- For dc analysis, open all the capacitance.

In the fig. shown, the single power source (for example, battery) is used for both collector and base of a transistor, although separate batteries can also be used.

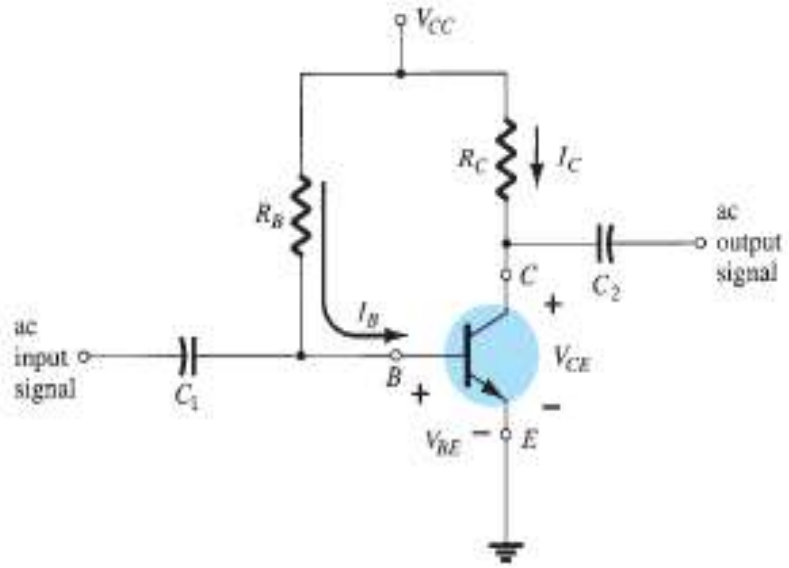


FIG. 4.2
Fixed-bias circuit.

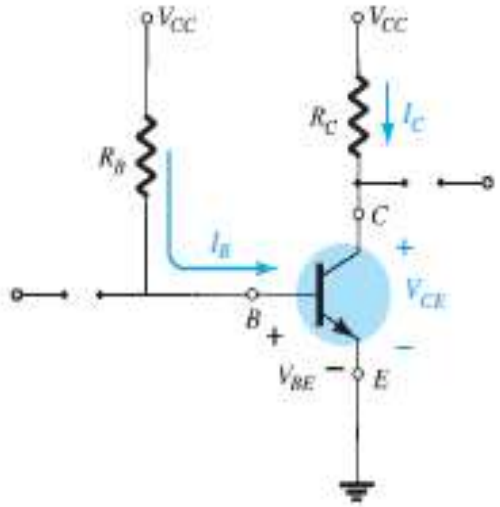


FIG. 4.3
DC equivalent of Fig. 4.2.

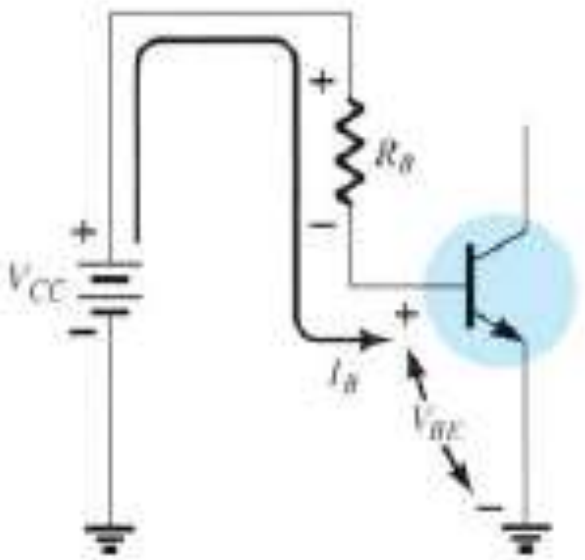


FIG. 4.4
Base–emitter loop.

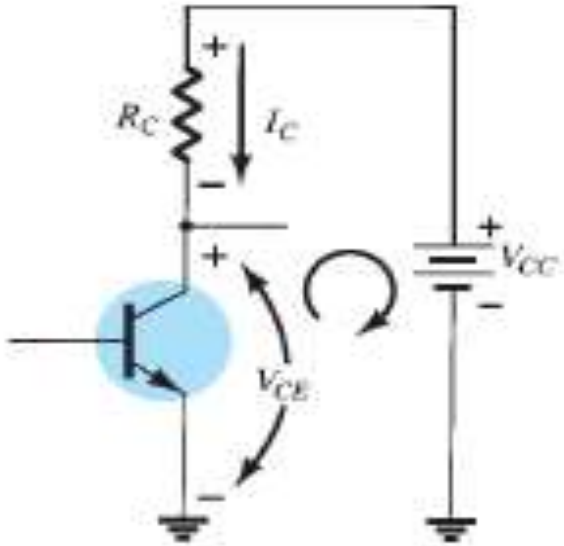


FIG. 4.5
Collector–emitter loop.

DC Analysis

- Applying KVL to the input loop: $+V_{CC} - I_B R_B - V_{BE} = 0$

$$V_{CC} = I_B R_B + V_{BE}$$

- From the above equation, deriving for IB, we get,

$$I_B = [V_{CC} - V_{BE}] / R_B$$

- The selection of R_B sets the level of base current for the operating point.
- Applying KVL for the output loop: $V_{CE} + I_C R_C - V_{CC} = 0$

$$V_{CC} = I_C R_C + V_{CE}$$

- Thus,

$$V_{CE} = V_{CC} - I_C R_C$$

- In circuits where emitter is grounded,

$$V_{CE} = V_E$$
$$V_{BE} = V_B$$

Design and Analysis

- **Design**: Given – I_B, I_C , V_{CE} and V_{CC}, or I_C , V_{CE} and β, design the values of R_B, R_C using the equations obtained by applying KVL to input and output loops.
- **Analysis**: Given the circuit values (V_{CC}, R_B and R_C), determine the values of I_B, I_C , V_{CE} using the equations obtained by applying KVL to input and output loops.

- When the transistor is biased such that I_B is very high so as to make I_C very high such that $I_C R_C$ drop is almost V_{CC} and V_{CE} is almost 0, the transistor is said to be in saturation.

$$I_C \text{ sat} = V_{CC} / R_C \quad \text{in a fixed bias circuit.}$$

Verification

- Whenever a fixed bias circuit is analyzed, the value of I_{CQ} obtained could be verified with the value of I_{CSat} ($= V_{CC} / R_C$) to understand whether the transistor is in active region.
- In active region,

$$I_{CQ} = (I_{CSat} /2)$$

Merits:

- It is simple to shift the operating point anywhere in the active region by merely changing the base resistor (RB).
- A very small number of components are required.

Demerits:

- The collector current does not remain constant with variation in temperature or power supply voltage. Therefore the operating point is unstable.
- When the transistor is replaced with another one, considerable change in the value ofß can be expected. Due to this change the operating point will shift.

- **Emitter Bias**

• It can be shown that, including an emitter resistor in the fixed bias circuit improves the stability of Q point.

• Thus emitter bias is a biasing circuit very similar to fixed bias circuit with an emitter resistor added to it.

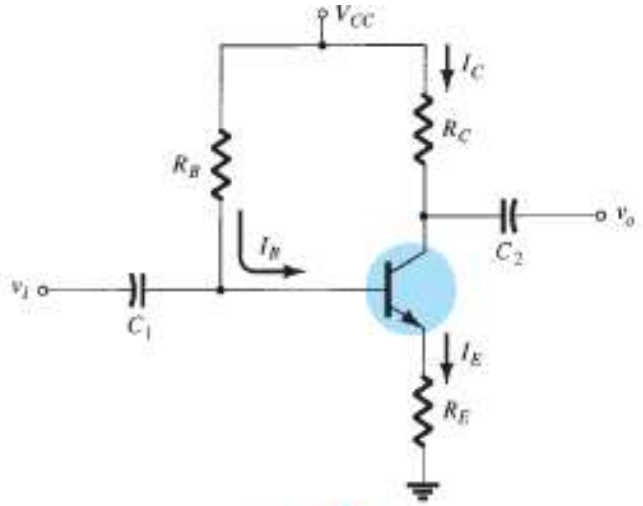


FIG. 4.17
BJT bias circuit with emitter resistor.

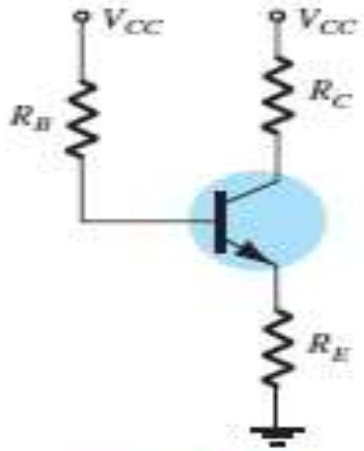


FIG. 4.18
DC equivalent of Fig. 4.17.

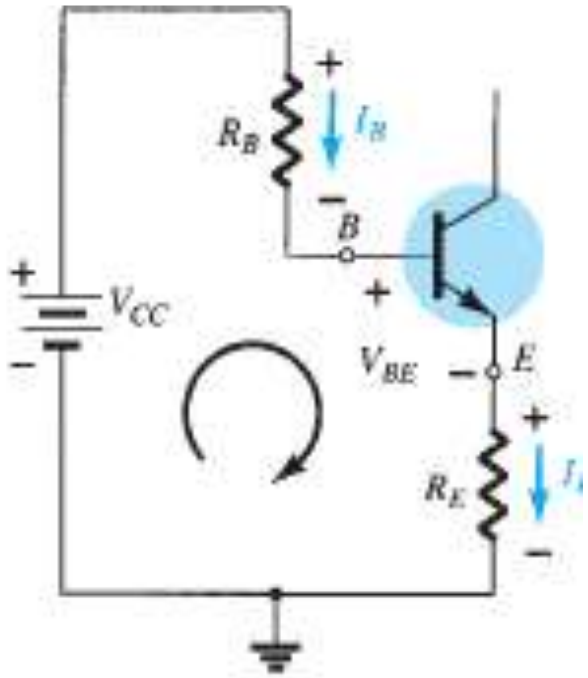


FIG. 4.19
Base–emitter loop.

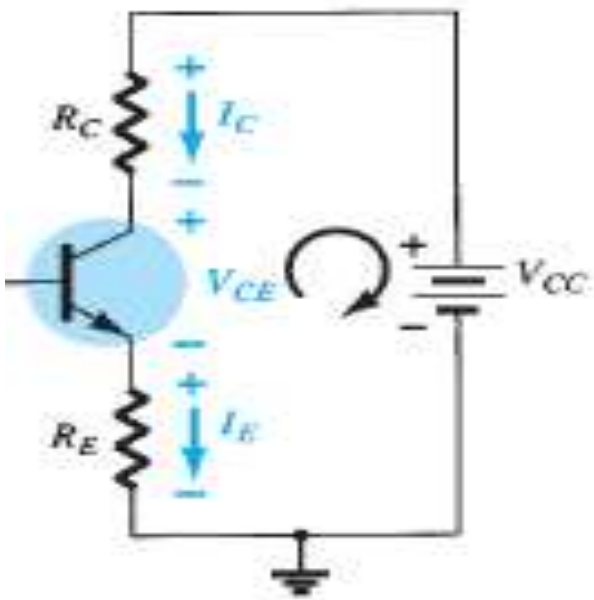


FIG. 4.22
Collector–emitter loop.

- Writing KVL around the input loop we get,

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E \quad (1)$$

We know that,

$$I_E = (\beta+1) I_B \quad (2)$$

Substituting this in (1), we get,

$$V_{CC} = I_B R_B + V_{BE} + (\beta+1) I_B R_E$$

$$V_{CC} - V_{BE} = I_B (R_B + (\beta+1) R_E)$$

Solving for I_B:

$$I_B = (V_{CC} - V_{BE}) / [(R_B + (\beta+1) R_E)]$$

The expression for I_B in a fixed bias circuit was,

$$I_B = (V_{CC} - V_{BE}) / R_B$$

- R_{EI} in the above circuit is $(\beta+1)R_E$ which means that, the emitter resistance that is common to both the loops appears as such a high resistance in the input loop.

- Thus $Ri = (\beta+1)R_E$ (more about this when we take up ac analysis)

Collector – emitter loop

Applying KVL,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

I_C is almost same as I_E

Thus,

$$V_{CC} = I_C R_C + V_{CE} + I_C R_E$$

$$= I_C (R_C + R_E) + V_{CE}$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Since emitter is not connected directly to ground, it is at a potential V_E, given by,

$$V_E = I_E R_E$$

$$V_C = V_{CE} + V_E \textbf{ OR } V_C = V_{CC} - I_C R_C$$

$$\text{Also, } V_B = V_{CC} - I_B R_B \textbf{ OR } V_B = V_{BE} + V_E$$

Improved bias stability

- Addition of emitter resistance makes the dc bias currents and voltages remain closer to their set value even with variation in
  - transistor beta
  - temperature

Stability

In a fixed bias circuit, I_B does not vary with β and therefore whenever there is an increase in β, I_C increases proportionately, and thus V_{CE} reduces making the Q point to drift towards saturation.In an emitter bias circuit, As β increases, I_B reduces, maintaining almost same I_C and V_{CE} thus stabilizing the Q point against β variations.

Saturation current

In saturation V_{CE} is almost 0V, thus

$$V_{CC} = I_C (R_C + R_E)$$

Thus, saturation current

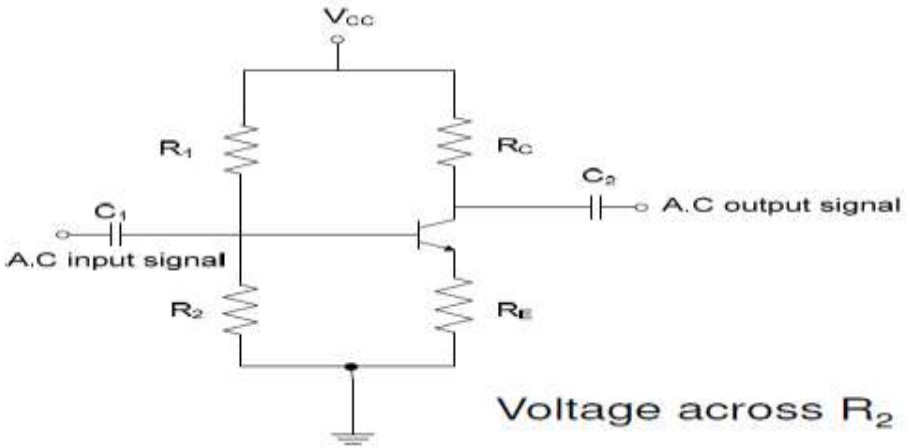
$$I_{C,sat} = V_{CC} / (R_C + R_E)$$

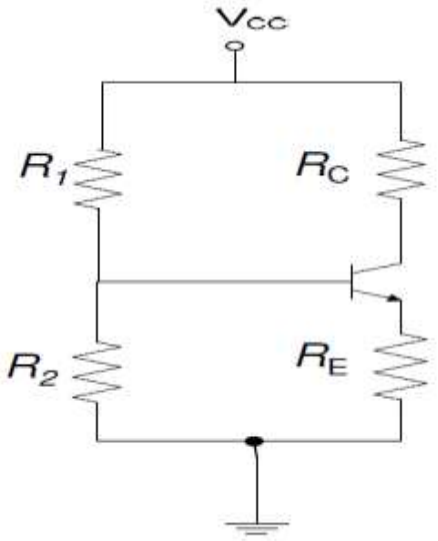
Contents of this Class:

- Self-bias circuit
- Collector Feedback bias circuit
- Bias Stabilization

Voltage divider bias (Self-bias circuit)

- This is the most widely used method to provide biasing and stabilization to a transistor.
- In this form of biasing, R_1 and R_2 divide the supply voltage V_{CC} and voltage across R_2 provide fixed bias voltage V_B at the transistor base.
- Also a resistance R_E is included in series with the emitter that provides the stabilization.
- The voltage divider as shown in the below figure is formed using external resistors R1 and R2. The voltage across R2 forward biases the emitter junction. By proper selection of resistors R1 and R2, the operating point of the transistor can be made independent of β. In this circuit, the voltage divider holds the base voltage fixed independent of base current provided the divider current is large compared to the base current. However, even with a fixed base voltage, collector current varies with temperature (for example) so an emitter resistor is added to stabilize the Q-point, similar to the above circuits with emitter resistor.

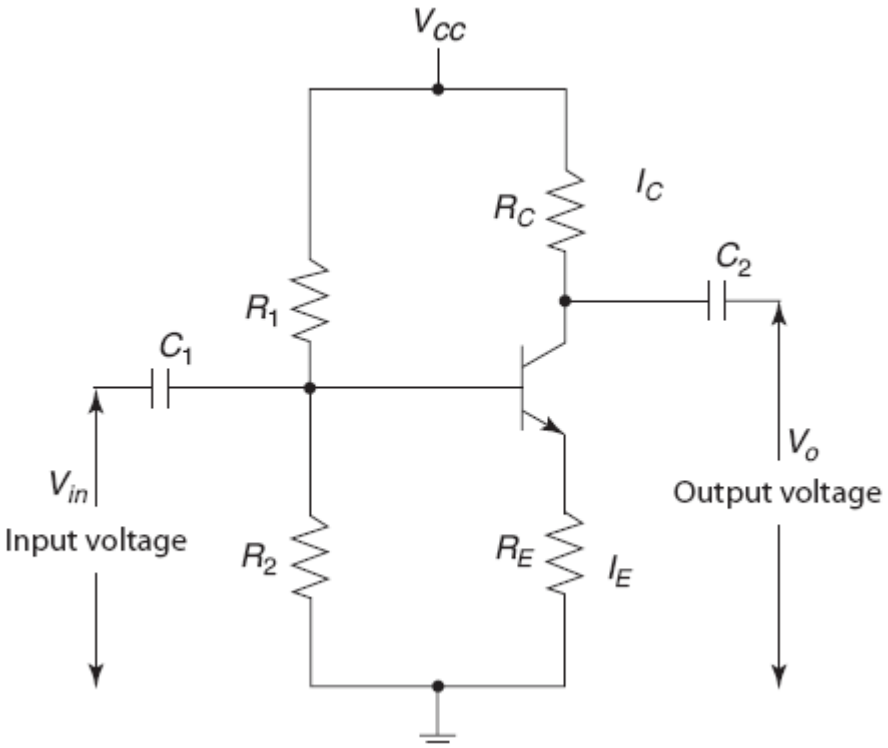




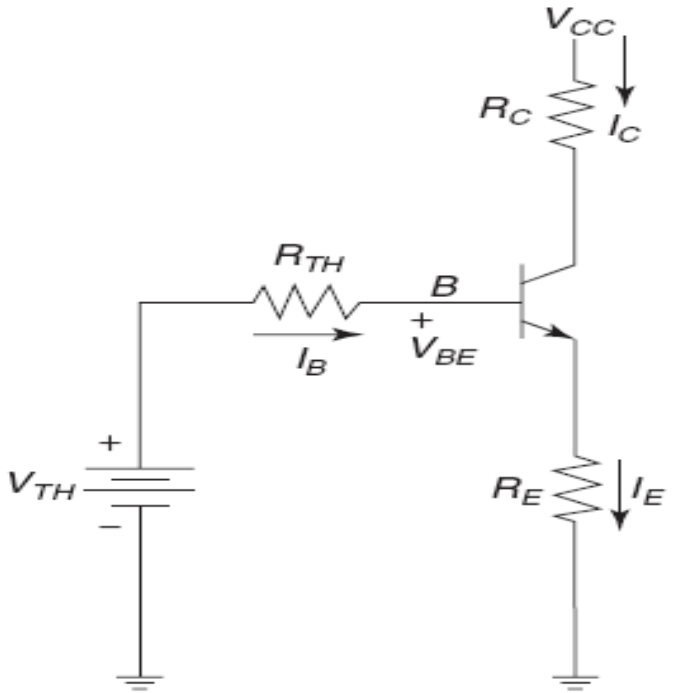
V_B = Voltage across R_2
(**ignoring base current**)

$$V_B = V_{CC}\frac{R_2}{(R_1 + R_2)}$$

Voltage divider bias (Self-bias circuit)



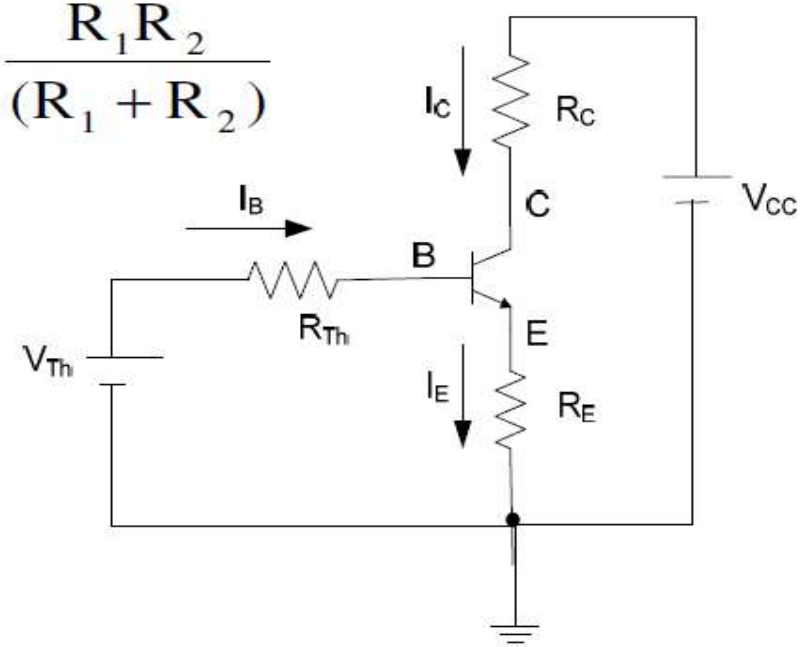
Voltage-divider bias circuit



Simplified voltage-divider circuit

Voltage Divider Bias

$$V_B = V_{Th} = V_{CC}\frac{R_2}{(R_1+R_2)} \qquad R_{Th} = R_1 \| R_2 = \frac{R_1 R_2}{(R_1+R_2)}$$



Base-Emitter Loop

$$V_{Th} - I_B R_{Th} - V_{BE} - (\beta+1) I_B R_E = 0$$

$$\text{or, } I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (\beta+1)R_E}$$

Collector- Emitter Loop

$$I_C = \beta I_B = \frac{\beta(V_{Th} - V_{BE})}{R_{Th} + (\beta+1)R_E} \qquad V_{CE} = V_{CC} - I_C R_C - I_E R_E = V_{CC} - I_C R_C - (I_C + I_B) R_E$$

For bais Stabilization : $R_{Th} << (\beta+1)R_E$

$$I_C \approx \frac{V_{Th} - V_{BE}}{R_E}$$

Voltage divider bias (Self-bias circuit)

- **Circuit recognition:** The voltage divider in the base circuit.
- **Advantages:** The circuit Q-point values are stable against changes in h_{FE}.
- **Disadvantages:** Requires more components than most other biasing circuits.
- **Applications:** Used primarily to bias linear amplifier.

Load line equations:

$$I_{C(\text{sat})} = \frac{V_{CC}}{R_C + R_E}$$

$$V_{CE(\text{off})} = V_{CC}$$

Q-point equations (assume that $h_{FE}R_E > 10R_2$):

$$V_B = V_{CC}\frac{R_2}{R_1 + R_2}$$

$$V_E = V_B - 0.7\text{V}$$

$$I_{CQ} \cong I_E = \frac{V_E}{R_E}$$

$$V_{CEQ} = V_{CC} - I_{CQ}\left(R_C + R_E\right)$$

Voltage divider bias (Self-bias circuit)

Merits:

- Unlike above circuits, only one dc supply is necessary.
- Operating point is almost independent of β variation.
- Operating point stabilized against shift in temperature.

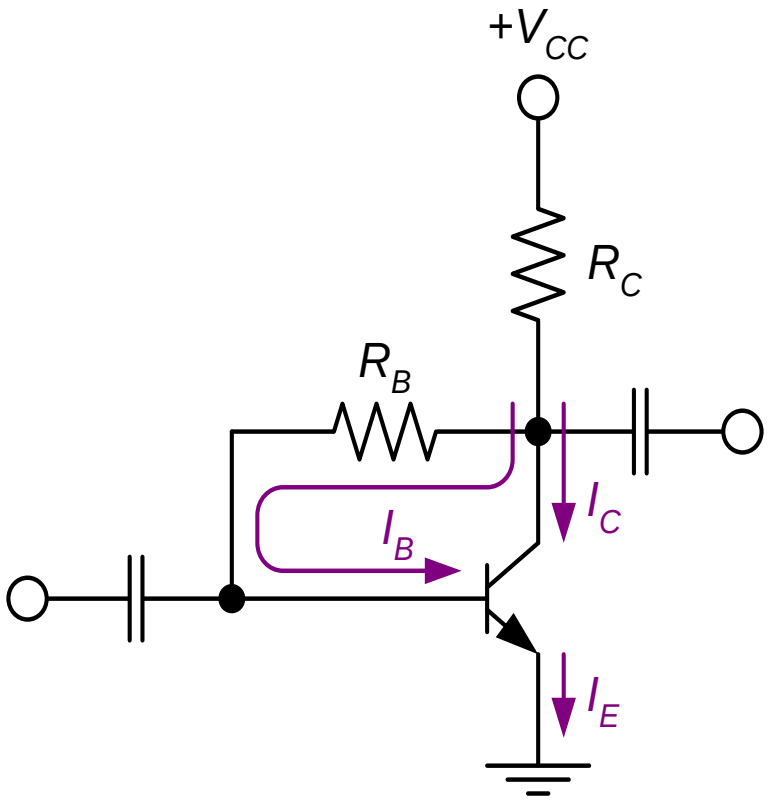
Demerits:

In this circuit, to keep IC independent of β the following condition must be met:

$$I_C = \beta I_B = \beta \frac{\frac{V_{CC}}{1+R_1/R_2} - V_{be}}{(\beta+1)R_E + R_1 \parallel R_2} \approx \frac{\frac{V_{CC}}{1+R_1/R_2} - V_{be}}{R_E},$$

which is approximately the case if $(\beta+1)R_E >> R_1 \parallel R_2$

Collector-feedback bias:



Circuit recognition: The base resistor is connected between the base and the collector terminals of the transistor.

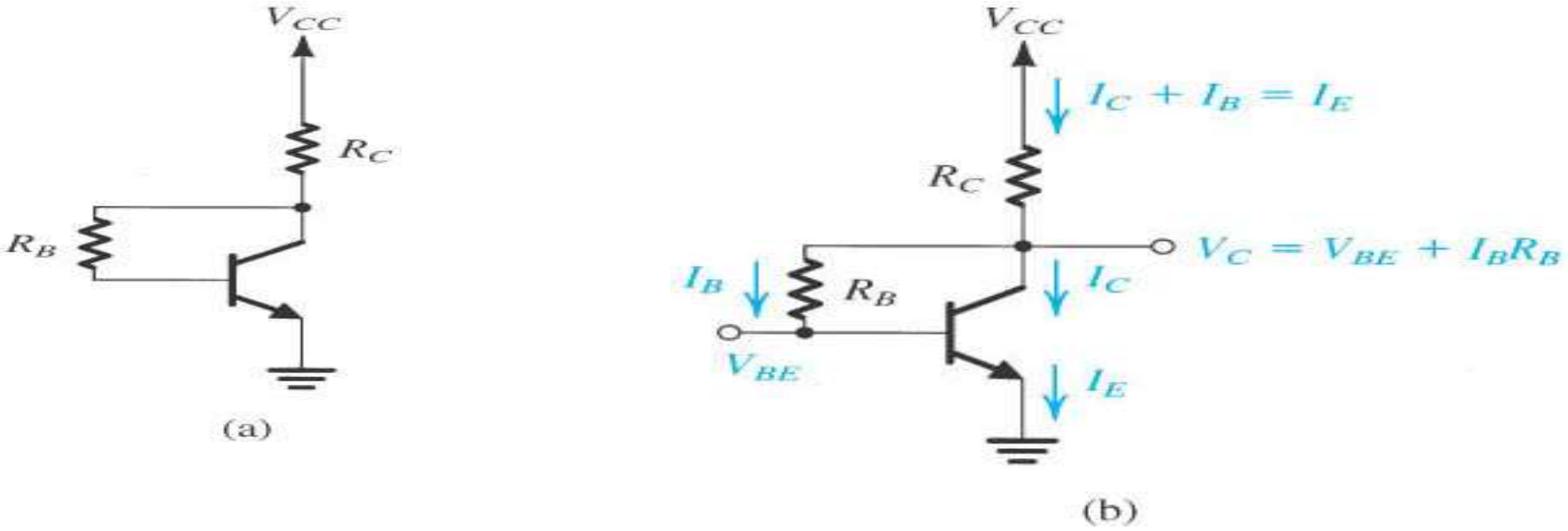
Advantage: A simple circuit with relatively stable Q-point.

Disadvantage: Relatively poor ac characteristics.

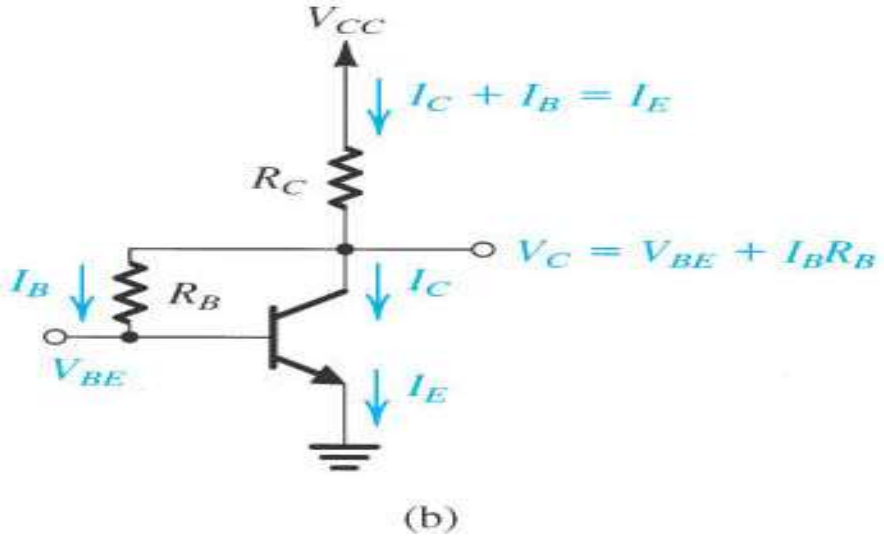
Applications: Used primarily to bias linear amplifiers.

Collector-feedback bias:

This configuration shown in figure employs negative feedback to prevent thermal runaway and stabilize the operating point. In this form of biasing, the base resistor R_B is connected to the collector instead of connecting it to the DC source Vcc. So any thermal runaway will induce a voltage drop across the R_C resistor that will throttle the transistor's base current.



Collector-feedback bias:



(b)

R_B provide negative Feedback

$$I_E = I_C + I_B$$

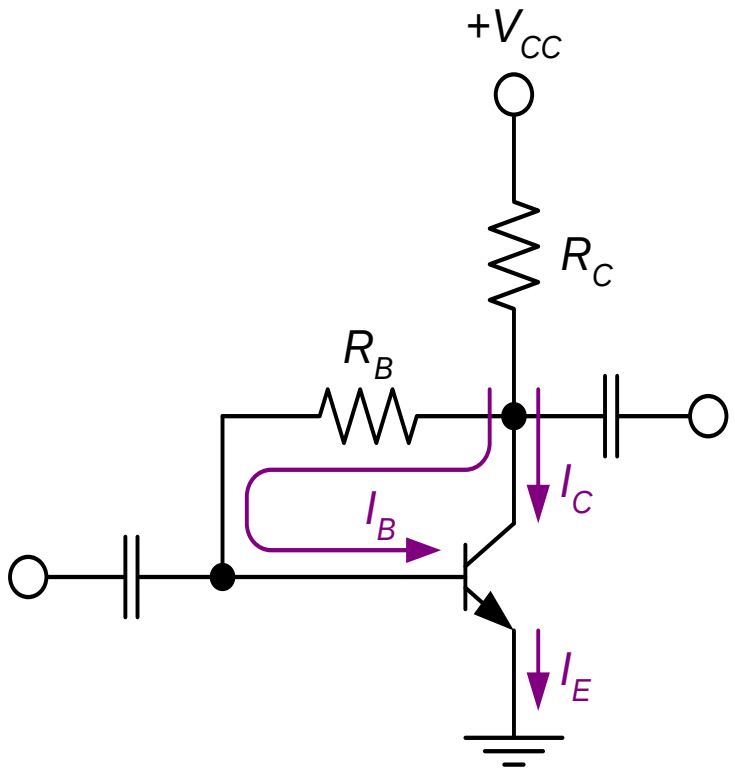
$$V_{CC} = I_E R_C + I_B R_B + V_{BE} \qquad I_B = \frac{I_E}{\beta + 1}$$

$$I_E = \frac{V_{CC} - V_{BE}}{R_C + \frac{R_B}{\beta + 1}}$$

$$V_{CC} >> V_{BE}$$

$$R_C >> \frac{R_B}{\beta + 1}$$

Collector-feedback bias:



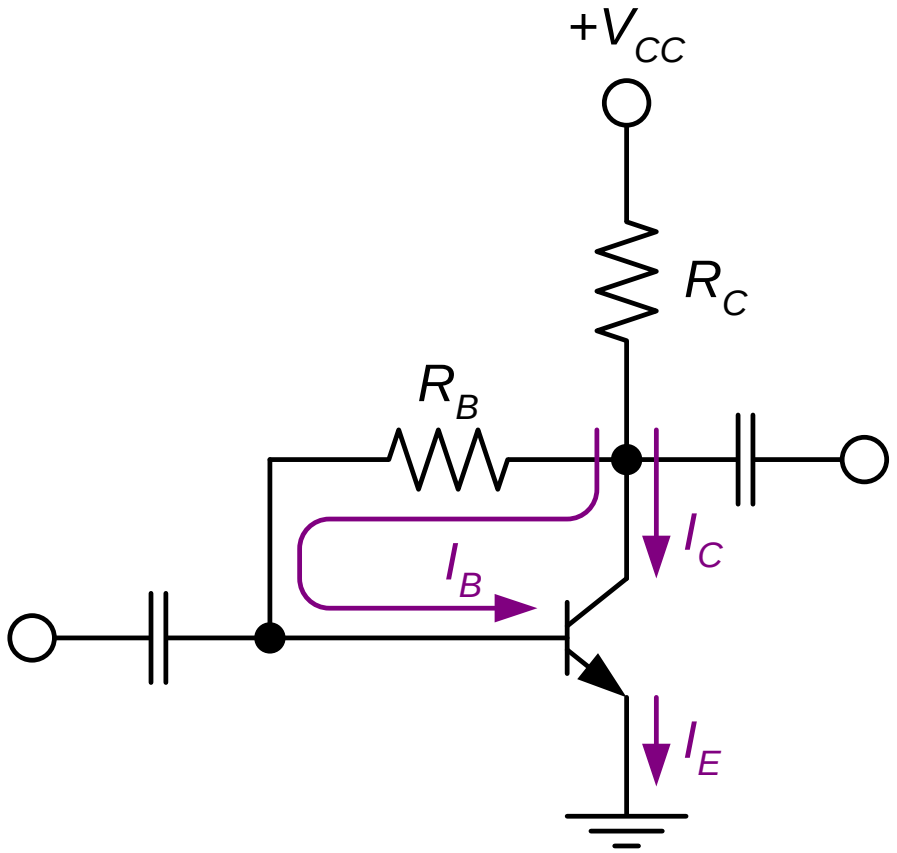
$$V_{CC} = \left(I_C + I_B\right)R_C + I_B R_B + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{(h_{FE} + 1)R_C + R_B}$$

$$I_{CQ} = h_{FE} I_B$$

$$V_{CEQ} = V_{CC} - \left(h_{FE} + 1\right) I_B R_C$$
$$\cong V_{CC} - I_{CQ} R_C$$

Collector-feedback bias:



Q-point relationships:

$$I_B = \frac{V_{CC} - V_{BE}}{(h_{FE} + 1)R_C + R_B}$$

$$I_{CQ} = h_{FE} I_B$$

$$V_{CEQ} \cong V_{CC} - I_{CQ} R_C$$

Collector-feedback bias:

Merits:

Circuit stabilizes the operating point against variations in temperature and β (i.e. replacement of transistor)

Demerits:

In this circuit, to keep Ic independent of β, the following condition must be met:

$$I_c = \beta I_b = \frac{\beta(V_{cc} - V_{be})}{R_b + R_c + \beta R_c} \approx \frac{(V_{cc} - V_{be})}{R_c}$$

which is the case when

$$\beta R_c \gg R_b.$$

Stabilization:

- **Biasing refers to the application of D.C. voltages to setup the operating point in such a way that output signal is undistorted throughout the whole operation.**
- **Also once selected properly, the Q point should not shift because of change of Ic due to**

(i) variation due to replacement of the transistor of same type

(ii) Temperature variation

<u>Stabilization:</u>

The process of making operating point independent of temperature changes or variation in transistor parameters is known as stabilization.

Stabilization of operating point is necessary due to

- **Temperature dependence of Ic**
- **Individual variations**
- **Thermal runaway**

- **Temperature dependence of I_C & Thermal runaway**

$$I_C = \beta I_B + (\beta + 1) I_{CBO}$$

- **I_{CBO} is strong function of temperature. A rise of 10 oC doubles the I_{CBO} and I_C will increase (β+1) times of I_{CBO}**
- **The flow of I_C produce heat within the transistor and raises the transistor temperature further and therefore, further increase in I_{CBO}**
- **This effect is cumulative and in few seconds, the I_C may become large enough to burn out the transistor.**
- **The self destruction of an unstablized transistor is known as thermal runaway.**

Stability Factor:

- **The rate of change collector current I_C with respect to the collector leakage current I_{CBO} at constant and I_B is called stability factor, denoted by S.**

$$I_C = \beta I_B + (\beta + 1) I_{CBO} \qquad (1)$$

Differentiating equation (1) w.r.t I_C

$$1 = \beta \left(\frac{dI_B}{dI_C}\right) + (\beta + 1) \frac{dI_{CBO}}{dI_C}$$

$$1 = \beta \left(\frac{dI_B}{dI_C}\right) + \frac{(\beta + 1)}{S}$$

$$S = \frac{(\beta + 1)}{1 - \beta \left(\frac{dI_B}{dI_C}\right)}$$

- **Stability Factor *S'*:-** The variation of I_C *with* V_{BE} *is given by the stability factor S defined by the partial derivative:*

$$S' \equiv \frac{\partial I_C}{\partial V_{BE}} \approx \frac{\Delta I_C}{\Delta V_{BE}}$$

❖ **Stability Factor *S″*:-** The variation of I_C *with respect to β is represented by the stability factor, S", given as:*

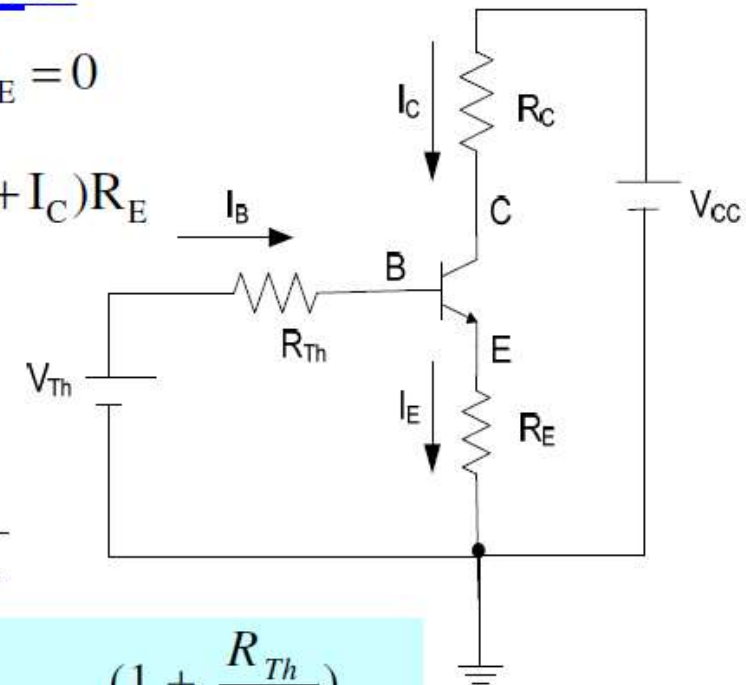
$$S'' \equiv \frac{\partial I_C}{\partial \beta} \approx \frac{\Delta I_C}{\Delta \beta}$$

Stability factor for Voltage Divider Bias

$$S = \frac{(\beta + 1)}{1 - \beta\left(\frac{dI_B}{dI_C}\right)}$$

$$V_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

(1) $$V_{Th} = I_B R_{Th} - V_{BE} - (I_B + I_C) R_E$$



Differentiating equation (1) w.r.t I_C

$$V_{Th} = I_B R_{Th} - V_{BE} - (I_B + I_C) R_E$$

$$0 = R_{Th}\left(\frac{dI_B}{dI_C}\right) + \left(1 + \frac{dI_B}{dI_C}\right) R_E$$

$$\frac{dI_B}{dI_C} = -\frac{R_E}{R_{Th} + R_E}$$

$$S = (\beta + 1)\frac{(R_{Th} + R_E)}{R_E(\beta + 1) + R_{Th}}$$

$$S = (\beta + 1)\frac{\left(1 + \frac{R_{Th}}{R_E}\right)}{(\beta + 1) + \frac{R_{Th}}{R_E}}$$

- For stability, S should be small which can be achieved by making R_{Th}/R_E small. For very small R_{Th}/R_E ; S = 1 (ideal case)

Thank You.

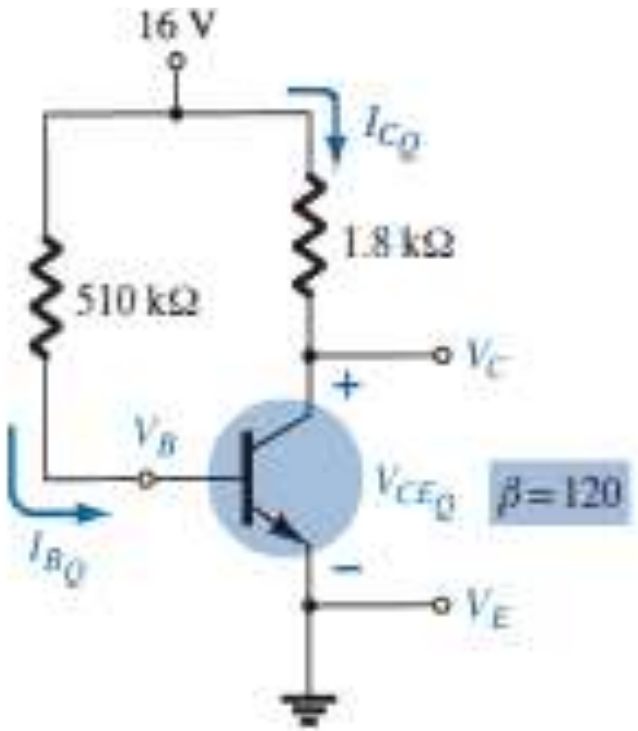
Contents of the Class:

- **Problems** on fixed bias, emitter bias, voltage divider bias and collector feedback bias.

Problem:1

For the given fixed bias circuit determine

a. I_{B_Q}.
b. I_{C_Q}.
c. V_{CE_Q}.
d. V_C.
e. V_B.
f. V_E.



Solution of Problem:1

(a) $$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{16\text{ V} - 0.7\text{ V}}{510\text{ k}\Omega} = \frac{15.3\text{ V}}{510\text{ k}\Omega} = \mathbf{30\ \mu A}$$

(b) $$I_{C_Q} = \beta I_{B_Q} = (120)(30\ \mu\text{A}) = \mathbf{3.6\ mA}$$

(c) $$V_{CE_Q} = V_{CC} - I_{C_Q} R_C = 16\text{ V} - (3.6\text{ mA})(1.8\text{ k}\Omega) = \mathbf{9.52\ V}$$

(d) $V_C = V_{CE_Q} =$ 9.52V

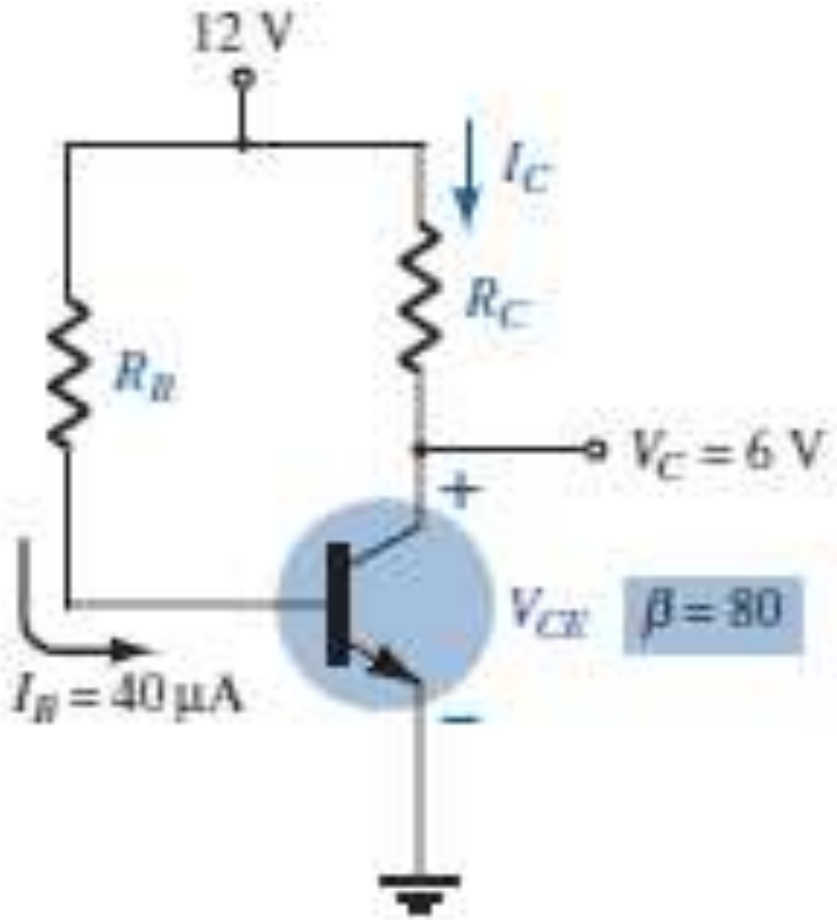
(e) $$V_B = V_{BE} = \mathbf{0.7\ V}$$

(f) $$V_E = \mathbf{0\ V}$$

Problem:2

For the given circuits determine

a. I_C.
b. R_C.
c. R_B.
d. V_{CE}.



Solution of Problem:2

(a) $I_C = \beta I_B = 80(40\ \mu\text{A}) = \mathbf{3.2\ mA}$

(b) $$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_C}{I_C} = \frac{12\ \text{V} - 6\ \text{V}}{3.2\ \text{mA}} = \frac{6\ \text{V}}{3.2\ \text{mA}} = \mathbf{1.875\ k\Omega}$$

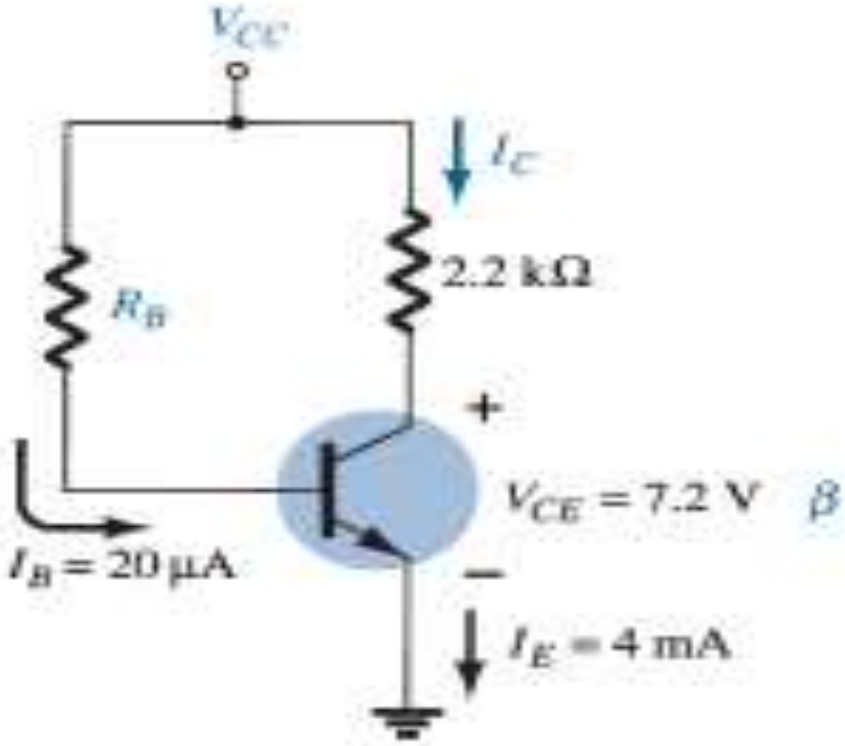
(c) $$R_B = \frac{V_{R_B}}{I_B} = \frac{12\ \text{V} - 0.7\ \text{V}}{40\ \mu\text{A}} = \frac{11.3\ \text{V}}{40\ \mu\text{A}} = \mathbf{282.5\ k\Omega}$$

(d) $V_{CE} = V_C = \mathbf{6\ V}$

Problem:3

For the given circuits determine

a. I_C.
b. V_{CC}.
c. β.
d. R_B.



Solution of Problem:3

(a) $I_C = I_E - I_B = 4\text{ mA} - 20\ \mu\text{A} = \mathbf{3.98\ mA} \cong 4\text{ mA}$

(b) $V_{CC} = V_{CE} + I_C R_C = 7.2\text{ V} + (3.98\text{ mA})(2.2\text{ k}\Omega)$

$= \mathbf{15.96\ V} \cong 16\text{ V}$

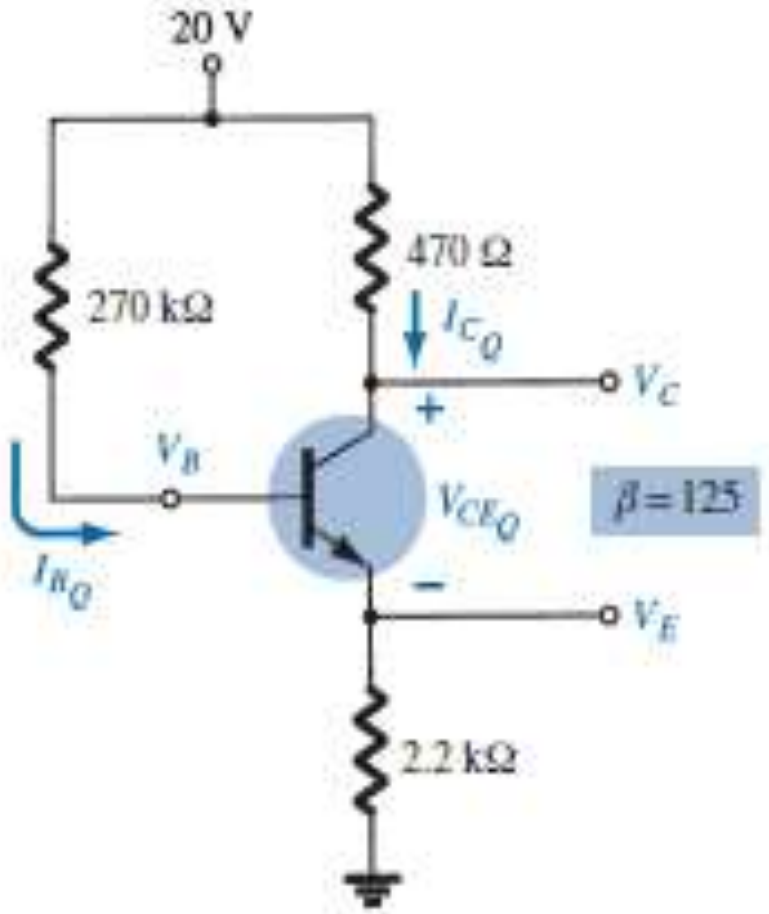
(c) $\beta = \dfrac{I_C}{I_B} = \dfrac{3.98\text{ mA}}{20\ \mu\text{A}} = \mathbf{199} \cong 200$

(d) $R_B = \dfrac{V_{R_B}}{I_B} = \dfrac{V_{CC} - V_{BE}}{I_B} = \dfrac{15.96\text{ V} - 0.7\text{ V}}{20\ \mu\text{A}} = \mathbf{763\ k\Omega}$

Problems:4

For emitter stabilized bias determines

a. I_{B_Q}
b. I_{C_Q}
c. V_{CE_Q}
d. V_C
e. V_B
f. V_E



Solution of Problem:4

(a) $$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{270\text{ k}\Omega + (126)2.2\text{ k}\Omega} = \frac{19.3\text{ V}}{547.2\text{ k}\Omega}$$
$$= \mathbf{35.27\ \mu A}$$

(b) $$I_{C_Q} = \beta I_{B_Q} = (125)(35.27\ \mu\text{A}) = \mathbf{4.41\ mA}$$

(c) $$V_{CE_Q} = V_{CC} - I_C(R_C + R_E) = 20\text{ V} - (4.41\text{ mA})(470\text{ k}\Omega + 2.2\text{ k}\Omega)$$
$$= 20\text{ V} - 11.77\text{ V}$$
$$= \mathbf{8.23\ V}$$

(d) $$V_C = V_{CC} - I_C R_C = 20\text{ V} - (4.41\text{ mA})(470\text{ k}\Omega) = 20\text{ V} - 2.07\text{ V}$$
$$= \mathbf{17.93\ V}$$

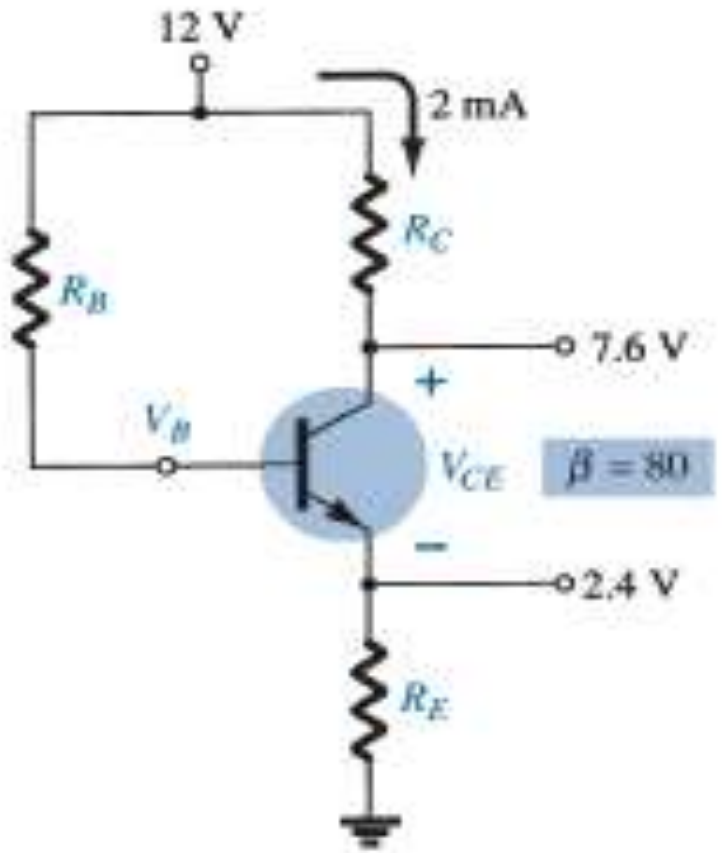
(e) $$V_B = V_{CC} - I_B R_B = 20\text{ V} - (35.27\ \mu\text{A})(270\text{ k}\Omega)$$
$$= 20\text{ V} - 9.52\text{ V} = \mathbf{10.48\ V}$$

(f) $$V_E = V_C - V_{CE} = 17.93\text{ V} - 8.23\text{ V} = \mathbf{9.7\ V}$$

Problem:5

For the given circuit determines

a. R_C.
b. R_E.
c. R_B.
d. V_{CE}.
e. V_B.



Solution of Problem:5

(a) $$R_C = \frac{V_{CC} - V_C}{I_C} = \frac{12\ \text{V} - 7.6\ \text{V}}{2\ \text{mA}} = \frac{4.4\ \text{V}}{2\ \text{mA}} = \mathbf{2.2\ k\Omega}$$

(b) $$I_E \cong I_C: \quad R_E = \frac{V_E}{I_E} = \frac{2.4\ \text{V}}{2\ \text{mA}} = \mathbf{1.2\ k\Omega}$$

(c) $$R_B = \frac{V_{R_B}}{I_B} = \frac{V_{CC} - V_{BE} - V_E}{I_B} = \frac{12\ \text{V} - 0.7\ \text{V} - 2.4\ \text{V}}{2\ \text{mA}/80} = \frac{8.9\ \text{V}}{25\ \mu\text{A}} = \mathbf{356\ k\Omega}$$

(d) $$V_{CE} = V_C - V_E = 7.6\ \text{V} - 2.4\ \text{V} = \mathbf{5.2\ V}$$

(e) $$V_B = V_{BE} + V_E = 0.7\ \text{V} + 2.4\ \text{V} = \mathbf{3.1\ V}$$

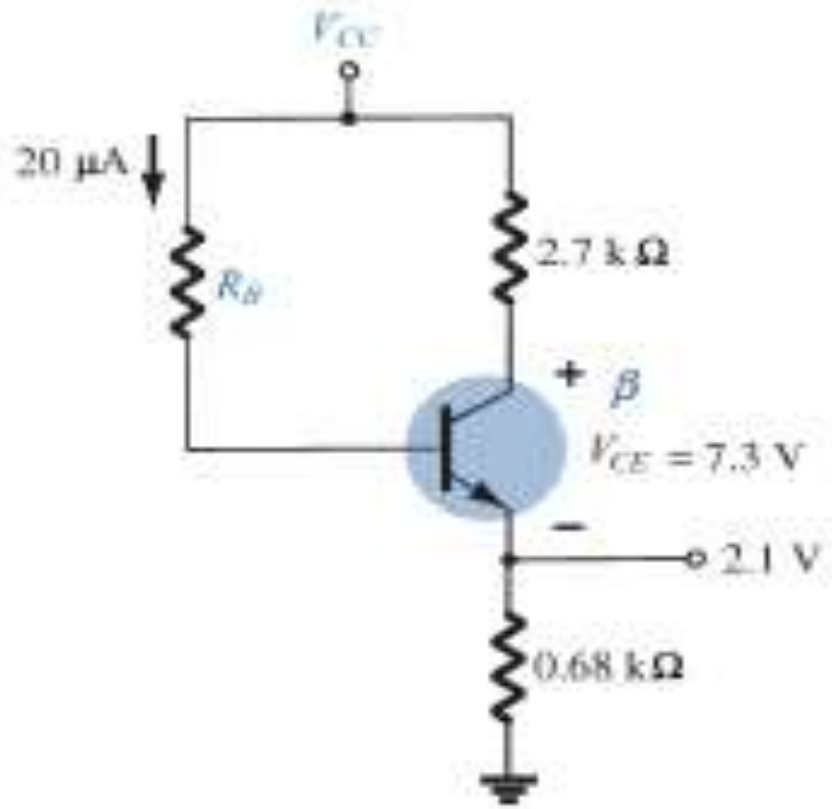
Problem:6

For the given circuit determines

a. β.

b. V_{CC}.

c. R_B.



Solution of Problem:6

(a) $$I_C \cong I_E = \frac{V_E}{R_E} = \frac{2.1\ \text{V}}{0.68\ \text{k}\Omega} = 3.09\ \text{mA}$$

$$\beta = \frac{I_C}{I_B} = \frac{3.09\ \text{mA}}{20\ \mu\text{A}} = \mathbf{154.5}$$

(b) $$V_{CC} = V_{R_C} + V_{CE} + V_E$$

$$= (3.09\ \text{mA})(2.7\ \text{k}\Omega) + 7.3\ \text{V} + 2.1\ \text{V} = 8.34\ \text{V} + 7.3\ \text{V} + 2.1\ \text{V}$$

$$= \mathbf{17.74\ V}$$

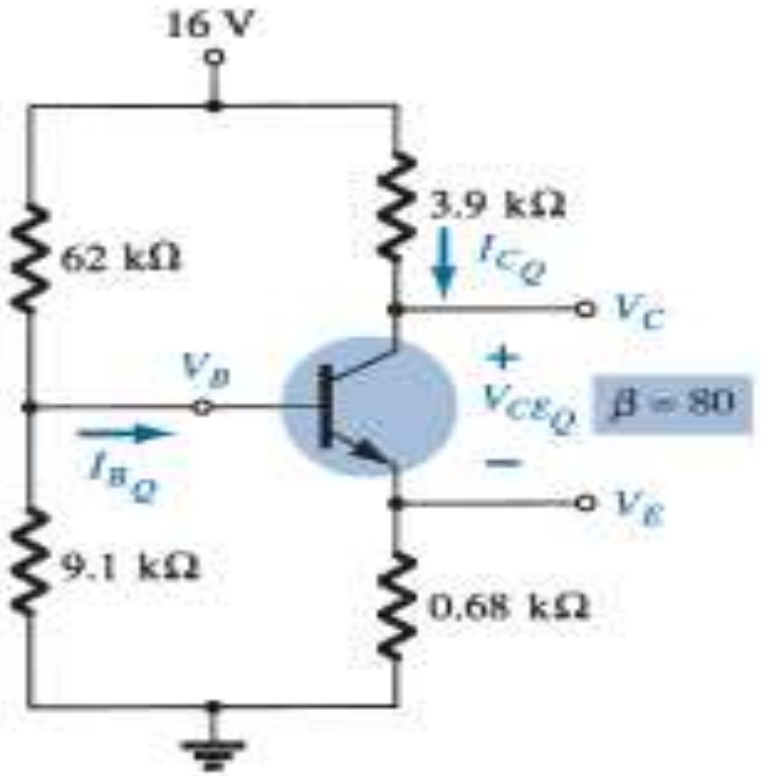
(c) $$R_B = \frac{V_{R_B}}{I_B} = \frac{V_{CC} - V_{BE} - V_E}{I_B} = \frac{17.74\ \text{V} - 0.7\ \text{V} - 2.1\ \text{V}}{20\ \mu\text{A}}$$

$$= \frac{14.94\ \text{V}}{20\ \mu\text{A}} = \mathbf{747\ k\Omega}$$

Problem:7

For the given voltage divider bias circuit determines

a. I_{B_Q}
b. I_{C_Q}
c. V_{CE_Q}
d. V_C
e. V_E
f. V_B



Solution of Problem:7

$$\beta R_E \geq 10R_2$$
$$(80)(0.68\ \text{k}\Omega) \geq 10(9.1\ \text{k}\Omega)$$
$$54.4\ \text{k}\Omega \not\geq 91\ \text{k}\Omega \text{ (No!)}$$

(a) Use exact approach:

$$R_{Th} = R_1 \parallel R_2 = 62\ \text{k}\Omega \parallel 9.1\ \text{k}\Omega = 7.94\ \text{k}\Omega$$

$$E_{Th} = \frac{R_2 V_{CC}}{R_2 + R_1} = \frac{(9.1\ \text{k}\Omega)(16\ \text{V})}{9.1\ \text{k}\Omega + 62\ \text{k}\Omega} = 2.05\ \text{V}$$

$$I_{B_Q} = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E} = \frac{2.05\ \text{V} - 0.7\ \text{V}}{7.94\ \text{k}\Omega + (81)(0.68\ \text{k}\Omega)}$$
$$= \mathbf{21.42\ \mu A}$$

(b) $I_{C_Q} = \beta I_{B_Q} = (80)(21.42\ \mu\text{A}) = \mathbf{1.71\ mA}$

(c) $V_{CE_Q} = V_{CC} - I_{C_Q}(R_C + R_E)$
$= 16\ \text{V} - (1.71\ \text{mA})(3.9\ \text{k}\Omega + 0.68\ \text{k}\Omega)$
$= \mathbf{8.17\ V}$

(d) $V_C = V_{CC} - I_C R_C$
$= 16\ \text{V} - (1.71\ \text{mA})(3.9\ \text{k}\Omega)$
$= \mathbf{9.33\ V}$

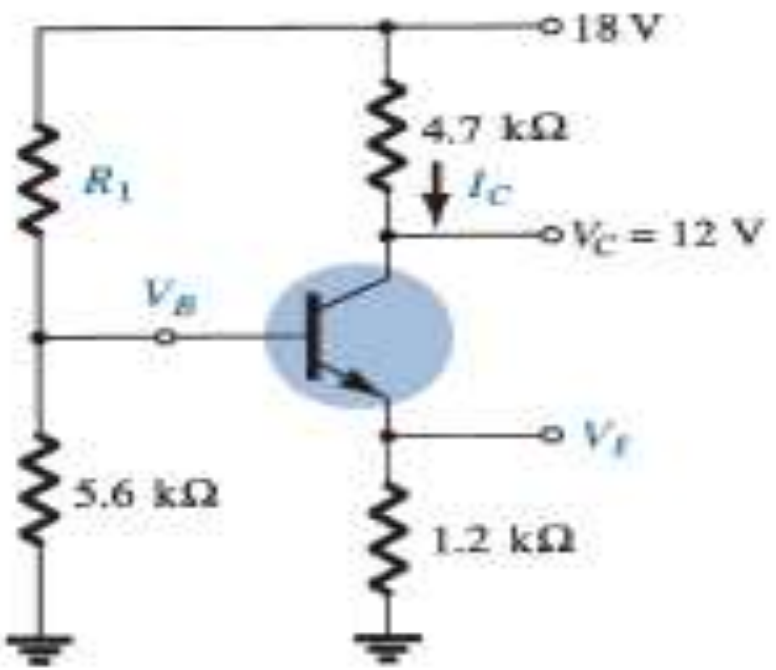
(e) $V_E = I_E R_E \cong I_C R_E = (1.71\ \text{mA})(0.68\ \text{k}\Omega)$
$= \mathbf{1.16\ V}$

(f) $V_B = V_E + V_{BE} = 1.16\ \text{V} + 0.7\ \text{V}$
$= \mathbf{1.86\ V}$

Problem:8

For the given voltage divider bias circuit determines

a. I_C.
b. V_E.
c. V_B.
d. R_1.



Solution of Problem:8

(a) $$I_C = \frac{V_{CC} - V_C}{R_C} = \frac{18\text{ V} - 12\text{ V}}{4.7\text{ k}\Omega} = \mathbf{1.28\text{ mA}}$$

(b) $$V_E = I_E R_E \cong I_C R_E = (1.28\text{ mA})(1.2\text{ k}\Omega) = \mathbf{1.54\text{ V}}$$

(c) $$V_B = V_{BE} + V_E = 0.7\text{ V} + 1.54\text{ V} = \mathbf{2.24\text{ V}}$$

(d) $$R_1 = \frac{V_{R_1}}{I_{R_1}}: \qquad V_{R_1} = V_{CC} - V_B = 18\text{ V} - 2.24\text{ V} = \mathbf{15.76\text{ V}}$$

$$I_{R_1} \cong I_{R_2} = \frac{V_B}{R_2} = \frac{2.24\text{ V}}{5.6\text{ k}\Omega} = 0.4\text{ mA}$$

$$R_1 = \frac{V_{R_1}}{I_{R_1}} = \frac{15.76\text{ V}}{0.4\text{ mA}} = \mathbf{39.4\text{ k}\Omega}$$

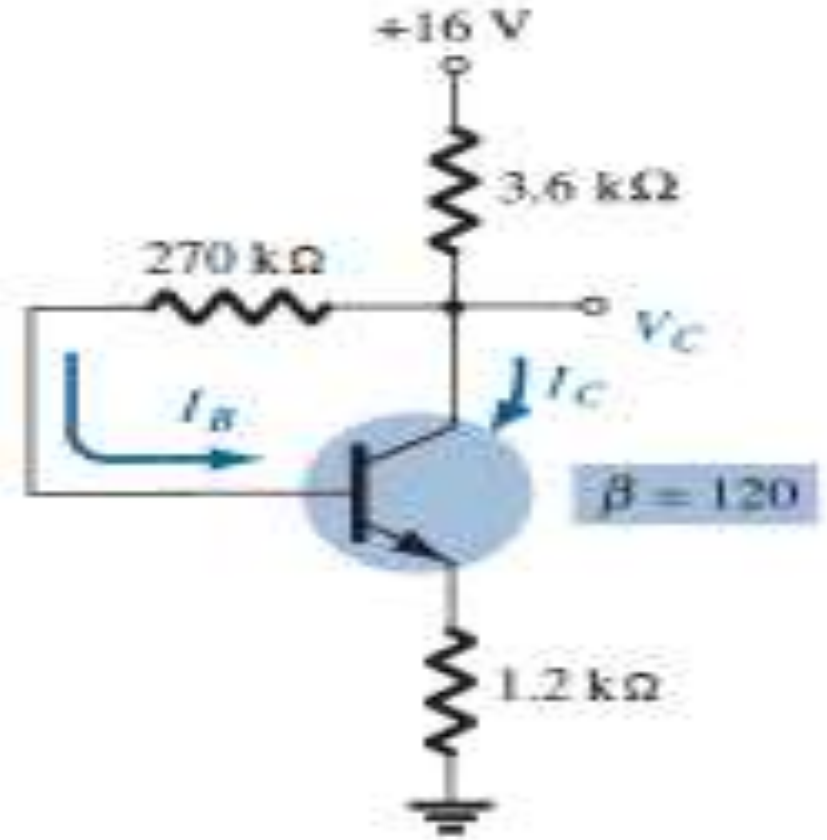
Problem:9

For the given collector feedback bias circuit determines

a. I_B.

b. I_C.

c. V_C.



Solution of Problem:9

$$\text{(a)}\quad I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)} = \frac{16\ \text{V} - 0.7\ \text{V}}{270\ \text{k}\Omega + (120)(3.6\ \text{k}\Omega + 1.2\ \text{k}\Omega)}$$

$$= \mathbf{18.09\ \mu A}$$

$$\text{(b)}\quad I_C = \beta I_B = (120)(18.09\ \mu\text{A})$$

$$= \mathbf{2.17\ mA}$$

$$\text{(c)}\quad V_C = V_{CC} - I_C R_C$$

$$= 16\ \text{V} - (2.17\ \text{mA})(3.6\ \text{k}\Omega)$$

$$= \mathbf{8.19\ V}$$

Thank You

Contents of the Class:

- AC analysis of Transistor
- Transistor Hybrid Model
- *h*- parameters
- Analysis of the transistor amplifier using *h*-parameter.

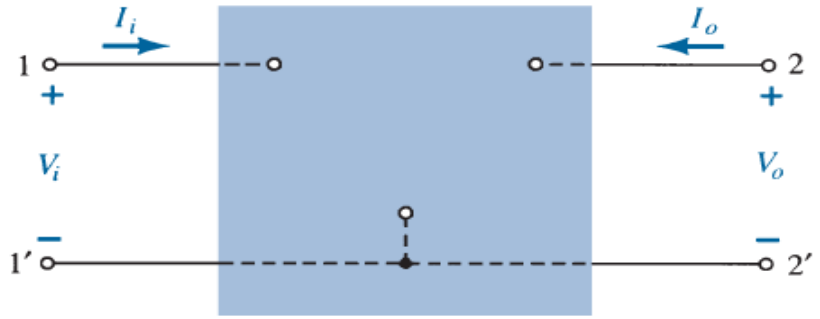
BJT Transistor modelling:
(ac analysis of BJT)

- A model is an equivalent circuit that represents the AC characteristics of the transistor.
- A model uses circuit elements that approximate the behavior of the transistor.
- There are 2 models commonly used in small signal AC analysis of a transistor:

i. r_e model
ii. Hybrid equivalent model

Two port device and hybrid model:

- For the hybrid equivalent model, the parameters are defined at an operating point.
- The quantities h_{ie},h_{re},h_{fe}, and h_{oe} are called hybrid parameters and are the components of a small – signal equivalent circuit.
- The description of the hybrid equivalent model will begin with the general two port system.



Two port System

$$V_i = h_{11}I_i + h_{12}V_o$$

$$I_o = h_{21}I_i + h_{22}V_o$$

- The parameters relating the four variables are called *h-parameters*, from the word “hybrid.” The term *hybrid* was chosen because the mixture of variables (*V* and *I*) in each equation results in a “hybrid” set of units of measurement for the *h*-parameters.

- The four variables h_{11}, h_{12}, h_{21} and h_{22} are called hybrid parameters (the mixture of variables in each equation results in a “hybrid” set of units of measurement for the h – parameters).
- h_{11}= h_i (input resistance)=$\left.{}^{V_i}/_{I_i}\right|_{V_o=0}$
- $h_{12} = h_r$(reversed voltage gain)=$\left.{}^{V_i}/_{V_o}\right|_{I_i=0}$
- $h_{21} = h_f$(forward current gain)=$\left.{}^{I_o}/_{I_i}\right|_{V_o=0}$
- $h_{22} = h_o$(output admittance)=$\left.{}^{I_o}/_{V_o}\right|_{I_i=0}$

Hybrid equivalent circuit:

$h_{11} \rightarrow$ *i*nput resistance $\rightarrow h_i$

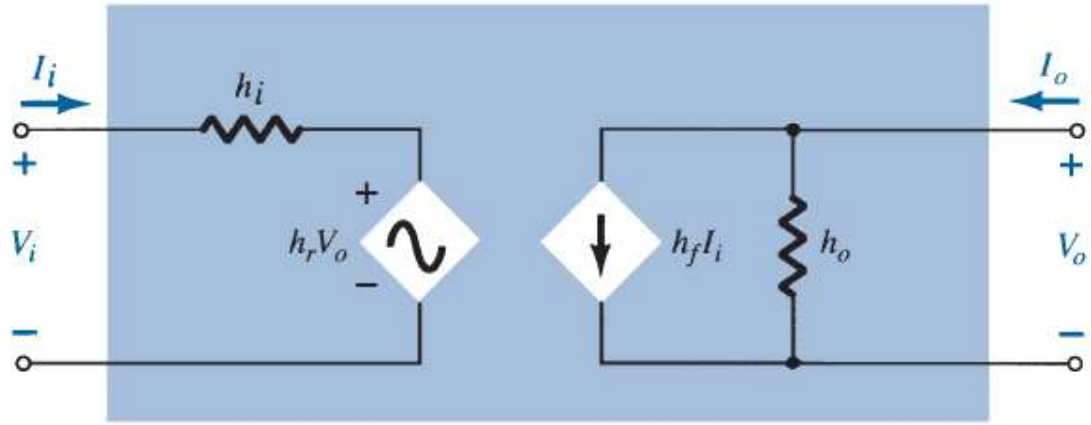
$h_{12} \rightarrow$ *r*everse transfer voltage ratio $\rightarrow h_r$

$h_{21} \rightarrow$ *f*orward transfer current ratio $\rightarrow h_f$

$h_{22} \rightarrow$ *o*utput conductance $\rightarrow h_o$

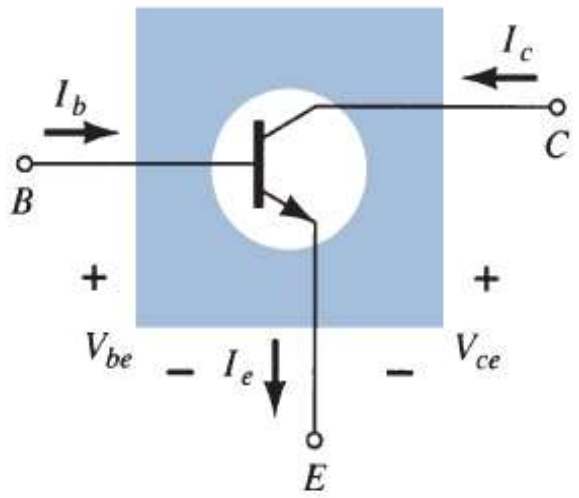
$$V_i = h_{11}I_i + h_{12}V_o$$

$$I_o = h_{21}I_i + h_{22}V_o$$

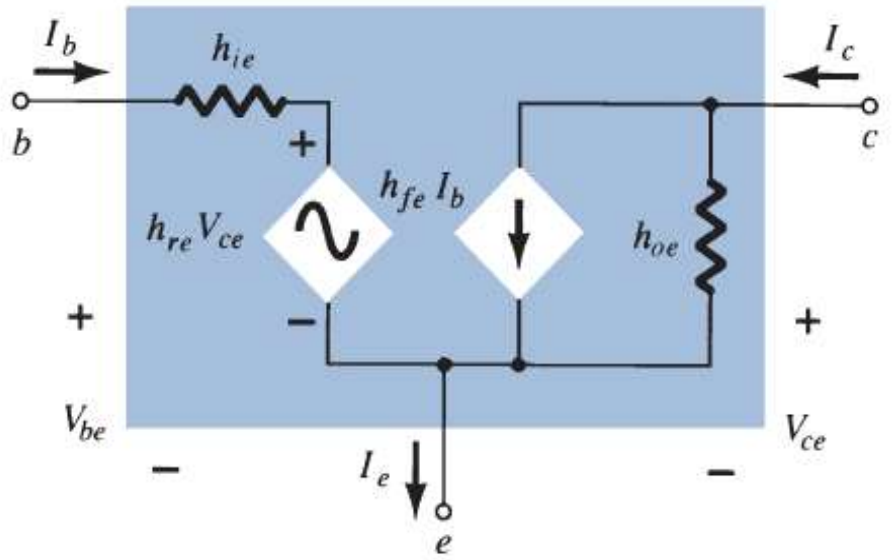


Hybrid Equivalent Circuit

Common Emitter Configuration:



(a)

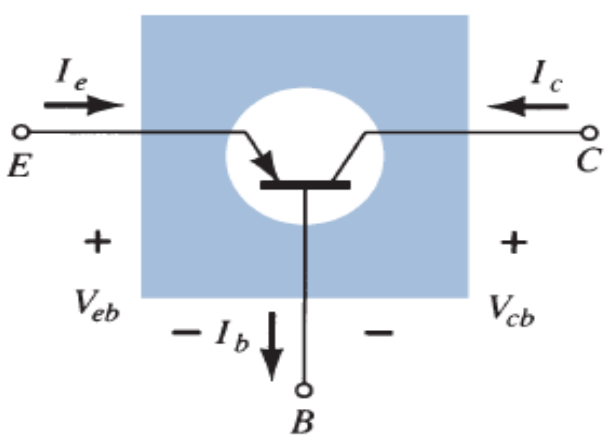


(b)

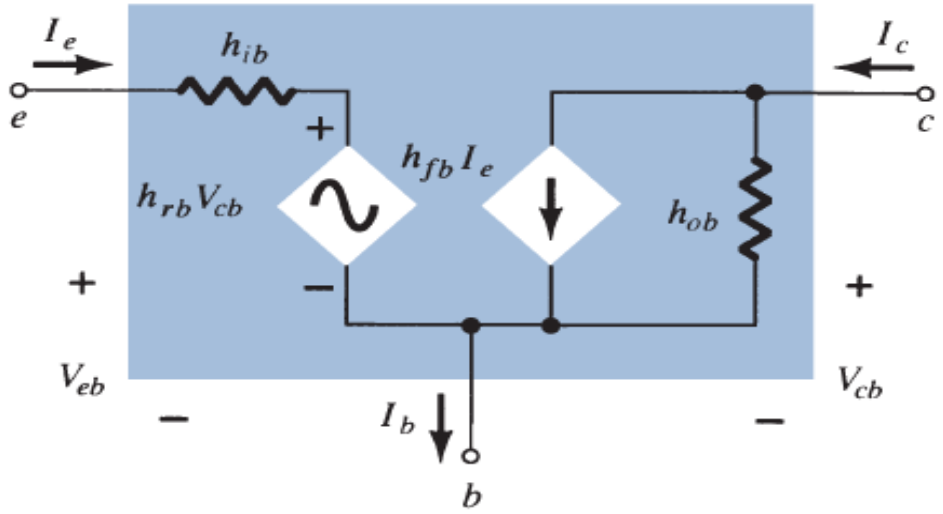
Graphical symbol

Hybrid Equivalent Circuit

Common Base Configuration:



(a)



(b)

Graphical Symbol

Hybrid Equivalent Circuit

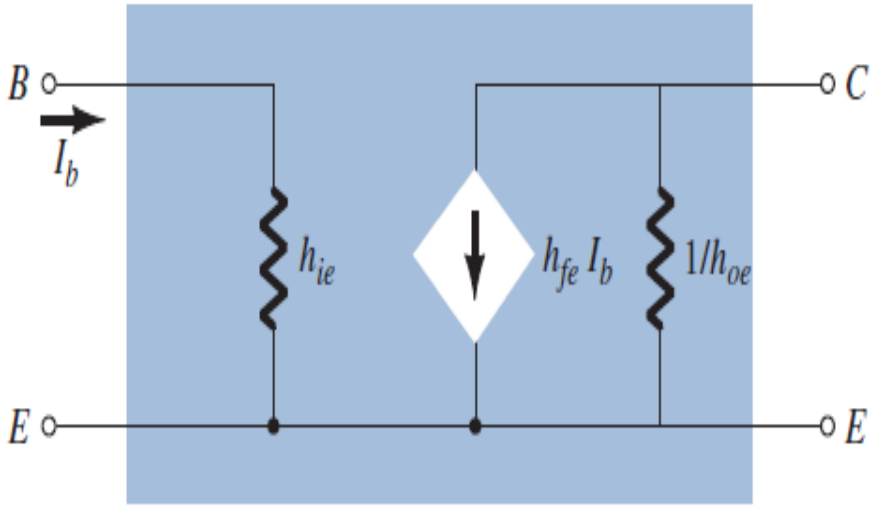
- Essentially, the transistor model is a three terminal two – port system.
- The h – parameters, however, will change with each configuration.
- To distinguish which parameter has been used or which is available, a second subscript has been added to the h – parameter notation.
- For the common – base configuration, the lowercase letter b is added, and for common emitter and common collector configurations, the letters e and c are used respectively

Configuration	I_i	I_o	V_i	V_o
Common emitter	I_b	I_c	V_{be}	V_{ce}
Common base	I_e	I_c	V_{eb}	V_{cb}
Common Collector	I_b	I_e	V_{be}	V_{ec}

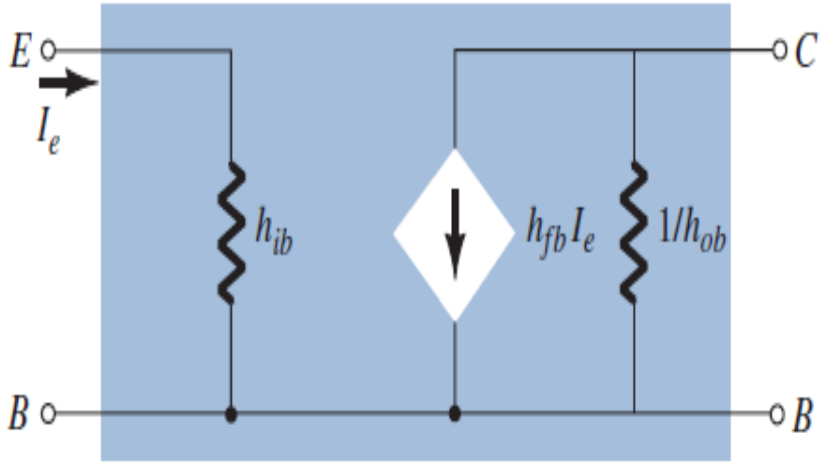
Input and output current and voltage of different transistor configuration in terms of h-parameter

- Normally h_r is a relatively small quantity, its removal is approximated by h_r and $h_r V_o = 0$, resulting in a short – circuit equivalent.
- The resistance determined by $1/h_0$ is often large enough to be ignored in comparison to a parallel load, permitting its replacement by an open – circuit equivalent.

Approximate Hybrid Equivalent Circuit:

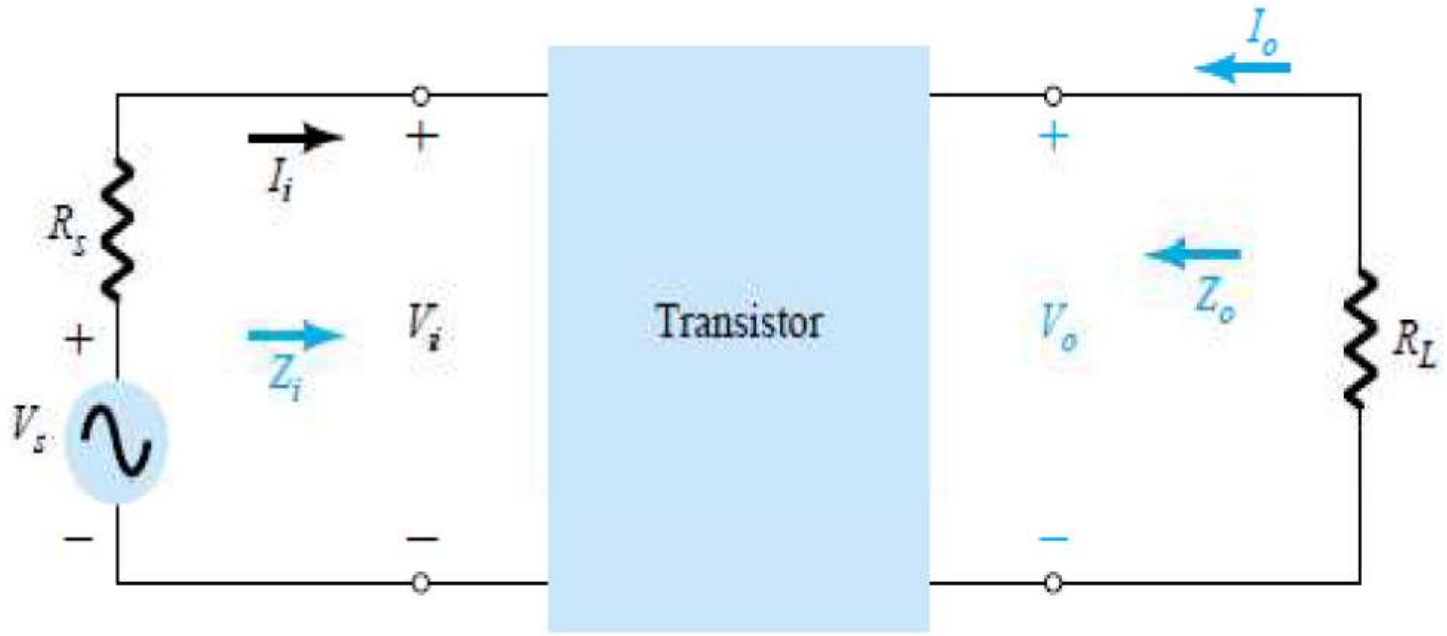


Approximate Common Emitter Hybrid Equivalent Circuit



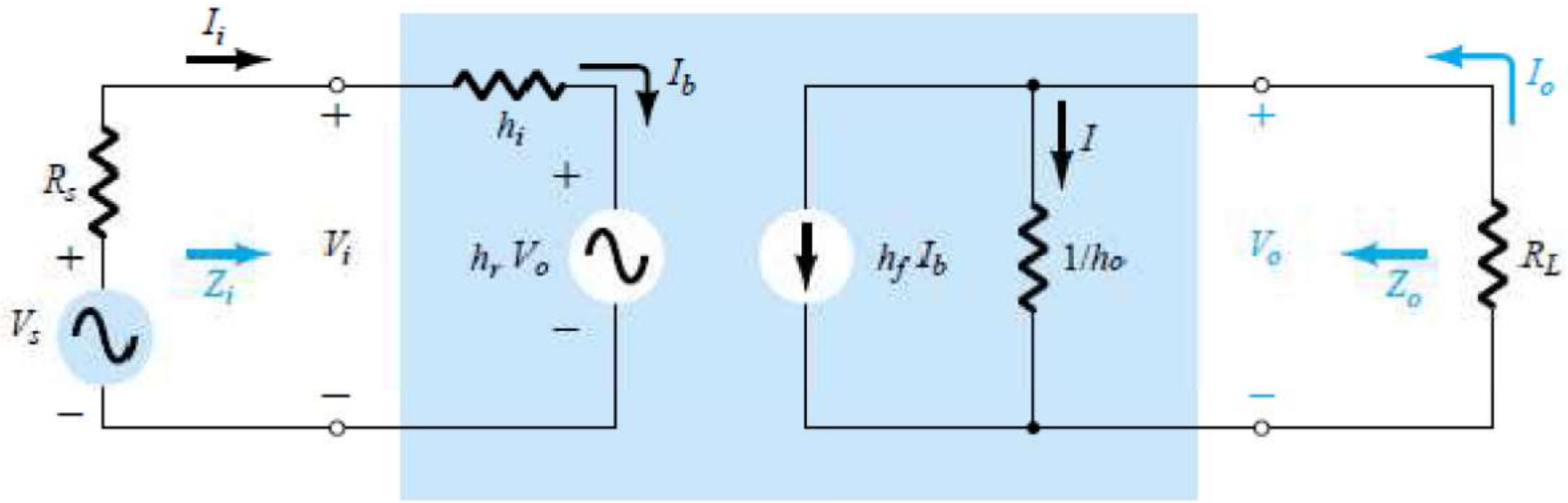
Approximate Common Base Hybrid Equivalent Circuit

Analysis of transistor amplifier using h-parameter:



Two-port system

Analysis of transistor amplifier using h-parameter:



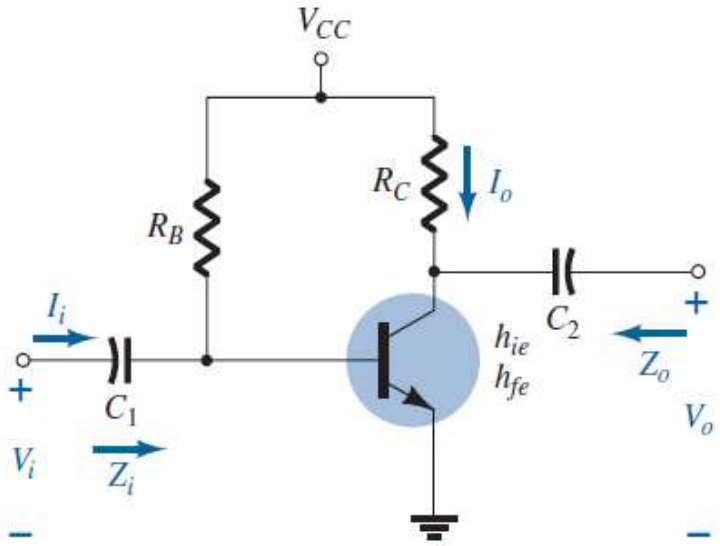
Substituting the complete hybrid equivalent circuit into the two-port system

Analysis of transistor amplifier using h-parameter:

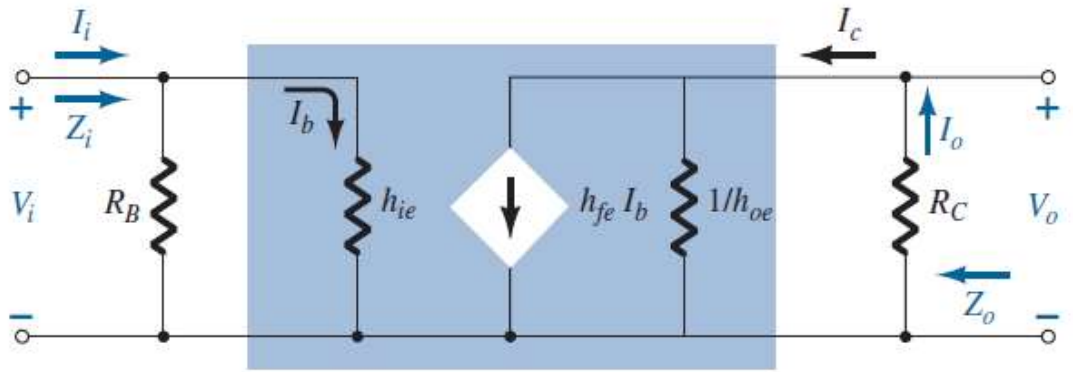
For analysis of transistor amplifier we have to determine the following terms:

- Current Gain(A_i)=I_o/I_i
- Voltage gain(A_V)=V_o/V_i
- Input impedance(Z_i)=V_i/I_i
- Output impedance(Z_o)=V_o/I_o

Fixed-bias Configuration(ac analysis):



Fixed bias configuration



Substituting the approximate hybrid equivalent circuit into the ac equivalent network

Z_i From Fig.

$$\boxed{Z_i = R_B \| h_{ie}}$$

Z_o From Fig.

$$\boxed{Z_o = R_C \| 1/h_{oe}}$$

A_v Using $R' = 1/h_{oe} \| R_C$, we obtain

$$V_o = -I_o R' = -I_C R'$$
$$= -h_{fe} I_b R'$$

and

$$I_b = \frac{V_i}{h_{ie}}$$

with

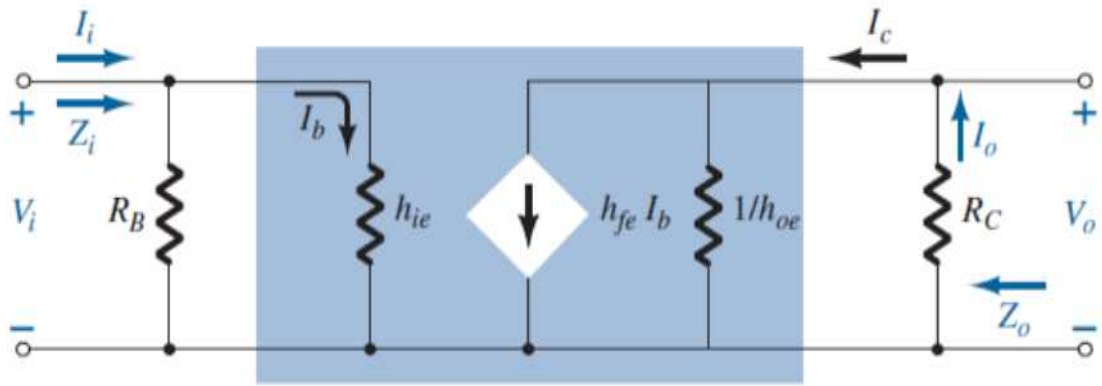
$$V_o = -h_{fe} \frac{V_i}{h_{ie}} R'$$

so that

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{h_{ie}(R_C \| 1/h_{oe})}{h_{ie}}}$$

A_i Assuming that $R_B \gg h_{ie}$ and $1/h_{oe} \geq 10R_C$, we find $I_b \cong I_i$ and $I_o = I_c = h_{fe} I_b = h_{fe} I_i$, and so

$$\boxed{A_i = \frac{I_o}{I_i} \cong h_{fe}}$$



EXAMPLE For the network of Fig. determine:

a. Z_i.
b. Z_o.
c. A_v.
d. A_i.

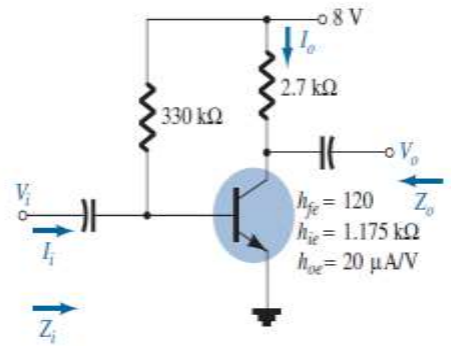
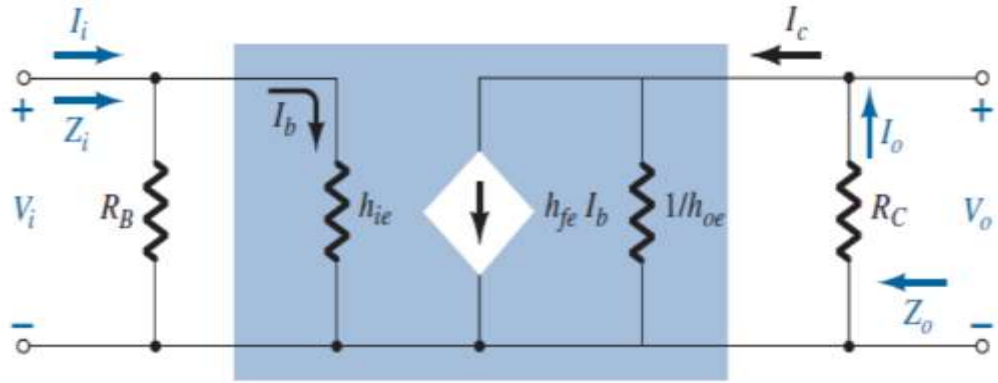


FIG.
Example



Solution:

a. $Z_i = R_B \| h_{ie} = 330\,\text{k}\Omega \| 1.175\,\text{k}\Omega$

$\cong h_{ie} = \mathbf{1.171\,k\Omega}$

b. $r_o = \dfrac{1}{h_{oe}} = \dfrac{1}{20\,\mu\text{A/V}} = 50\,\text{k}\Omega$

$Z_o = \dfrac{1}{h_{oe}} \| R_C = 50\,\text{k}\Omega \| 2.7\,\text{k}\Omega = \mathbf{2.56\,k\Omega} \cong R_C$

c. $A_v = -\dfrac{h_{fe}(R_C \| 1/h_{oe})}{h_{ie}} = -\dfrac{(120)(2.7\,\text{k}\Omega \| 50\,\text{k}\Omega)}{1.171\,\text{k}\Omega} = \mathbf{-262.34}$

d. $A_i \cong h_{fe} = \mathbf{120}$

Voltage-divider bias:

For the voltage-divider bias configuration the resulting small-signal ac equivalent network will have the same as fixed bias circuit, with R_B replaced by $R' = R_1 \| R_2$.

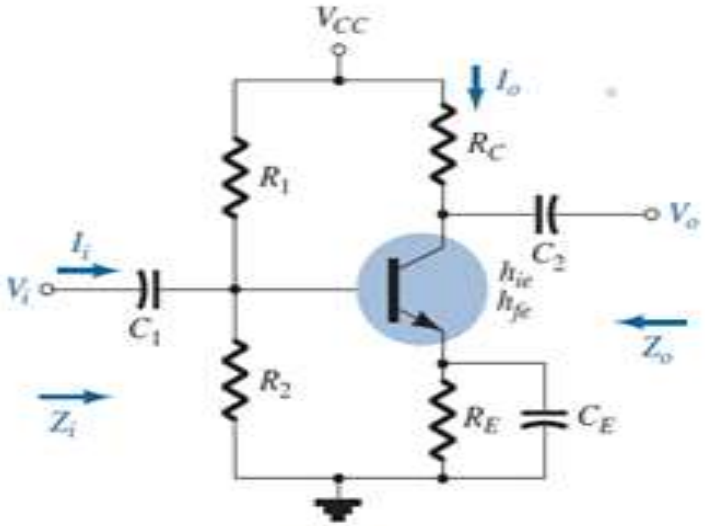
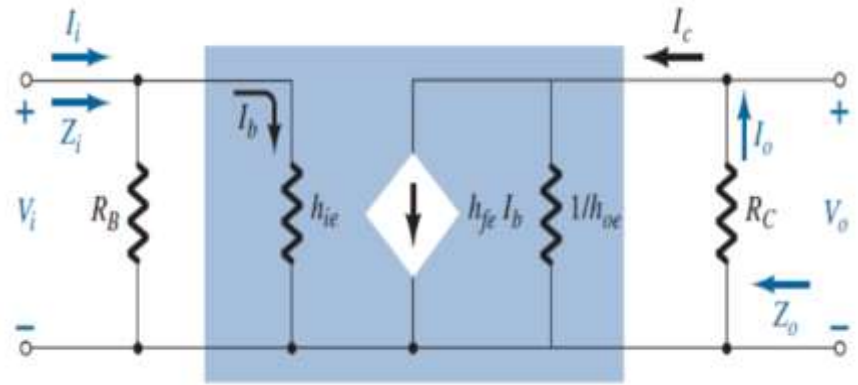


FIG.
Voltage-divider bias configuration.



Voltage-divider bias:

Z_i From Fig. with $R_B = R'$,

$$Z_i = R_1 \| R_2 \| h_{ie}$$

Z_o From Fig.

$$Z_o \cong R_C$$

A_v

$$A_v = -\frac{h_{fe}(R_C \| 1/h_{oe})}{h_{ie}}$$

A_i

$$A_i = \frac{h_{fe}(R_1 \| R_2)}{R_1 \| R_2 + h_{ie}}$$

CE emitter-bias Configuration using r_e model:

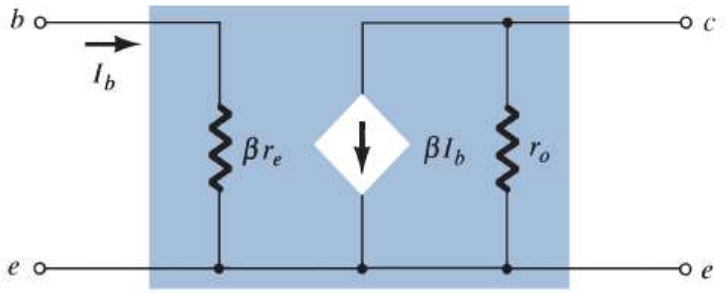
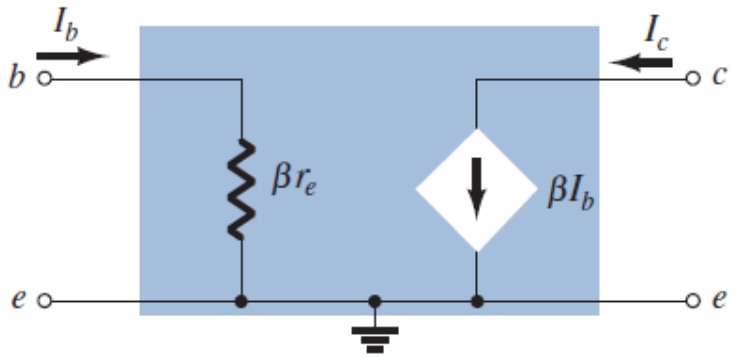


FIG.

r_e model for the common-emitter transistor configuration including effects of r_o.



r_e model without effect of r_o

CE emitter-bias Configuration using r_e model:

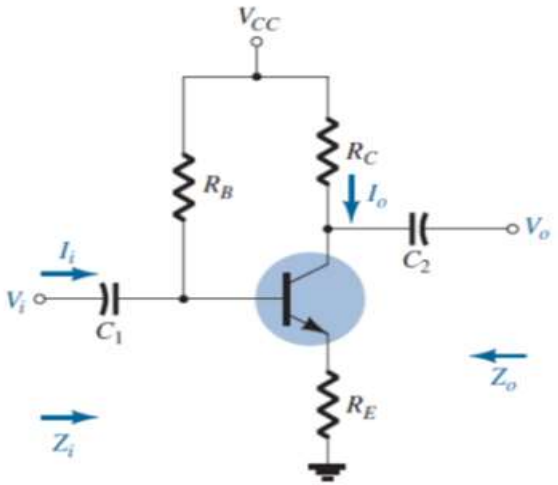


FIG. 1
CE emitter-bias configuration.

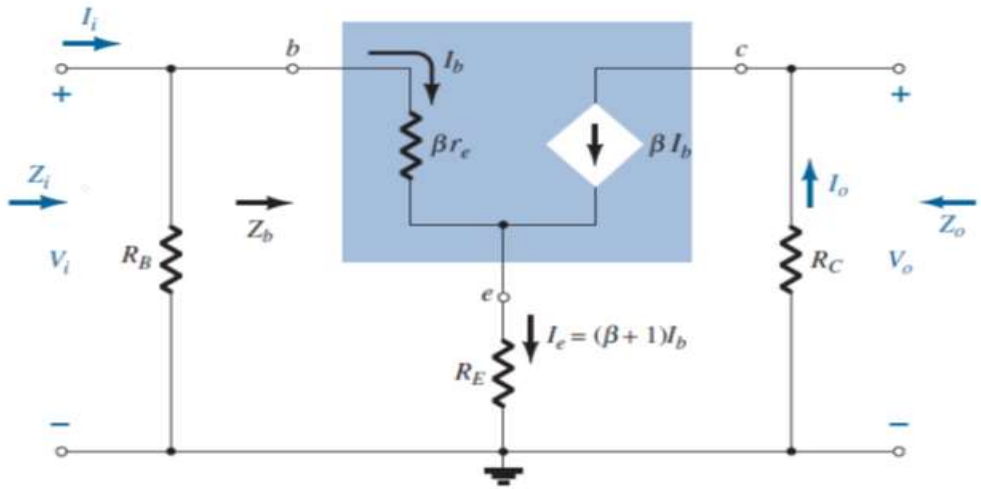


FIG. 2
Substituting the r_e equivalent circuit into the ac equivalent network

Applying Kirchhoff's voltage law to the input side of Fig. results in

$$V_i = I_b\beta r_e + I_e R_E$$

or

$$V_i = I_b\beta r_e + (\beta + I)I_b R_E$$

and the input impedance looking into the network to the right of R_B is

$$Z_b = \frac{V_i}{I_b} = \beta r_e + (\beta + 1)R_E$$

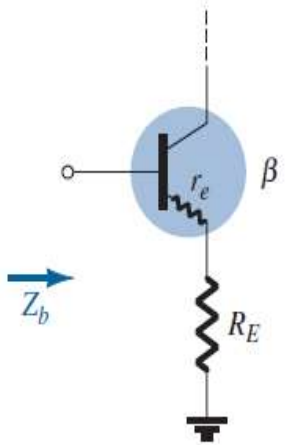


FIG. 3
Defining the input impedance of a transistor with an unbypassed emitter resistor.

The result as displayed in Fig. 3 reveals that the input impedance of a transistor with an unbypassed resistor R_E is determined by

$$\boxed{Z_b = \beta r_e + (\beta + 1)R_E}$$

Because β is normally much greater than 1, the approximate equation is

$$Z_b \cong \beta r_e + \beta R_E$$

and

$$\boxed{Z_b \cong \beta(r_e + R_E)}$$

Because R_E is usually greater than r_e, Eq. can be further reduced to

$$\boxed{Z_b \cong \beta R_E}$$

Z_i we have

$$\boxed{Z_i = R_B \| Z_b}$$

Z_o With V_i set to zero, $I_b = 0$, and βI_b can be replaced by an open-circuit equivalent. The result is

$$\boxed{Z_o = R_C}$$

A_v

$$I_b = \frac{V_i}{Z_b}$$

and

$$V_o = -I_o R_C = -\beta I_b R_C$$
$$= -\beta\left(\frac{V_i}{Z_b}\right)R_C$$

with

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{\beta R_C}{Z_b}}$$

Substituting $Z_b \cong \beta(r_e + R_E)$ gives

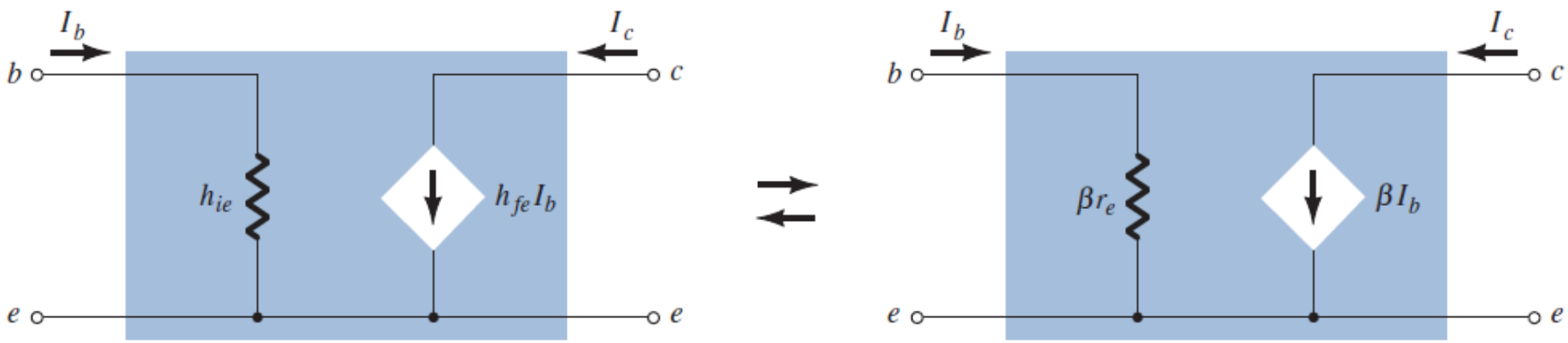
$$\boxed{A_v = \frac{V_o}{V_i} \cong -\frac{R_C}{r_e + R_E}}$$

and for the approximation $Z_b \cong \beta R_E$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong -\frac{R_C}{R_E}}$$

Note the absence of β from the equation for A_v demonstrating an independence in variation of β.

Relationship between r_e and hybrid model:



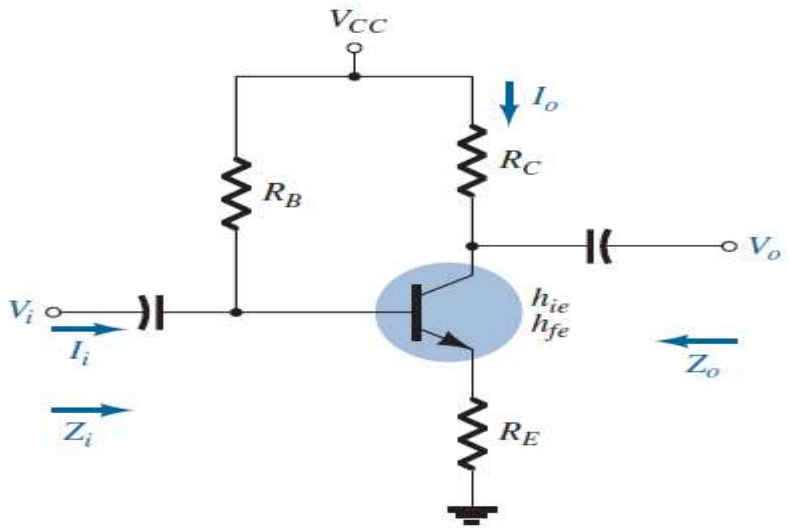
$$h_{ie} = \beta r_e$$

$$h_{fe} = \beta_{ac}$$

$$r_o = \frac{1}{h_{oe}}$$

Unbypassed emitter-bias Configuration analysis using Hybrid model:

- For the CE unbypassed emitter-bias configuration, the small-signal ac model will be the same as r_e model analysis , with βr_e replaced by h_{ie} and βI_b by $h_{fe} I_b$.
- The analysis will proceed in the same manner as r_e model analysis.



CE unbypassed emitter-bias configuration.

Unbypassed emitter-bias Configuration analysis using Hybrid model:

Z_i

$$Z_b \cong h_{fe} R_E$$

and

$$Z_i = R_B \| Z_b$$

Z_o

$$Z_o = R_C$$

A_v

$$A_v = -\frac{h_{fe} R_C}{Z_b} \cong -\frac{h_{fe} R_C}{h_{fe} R_E}$$

and

$$A_v \cong -\frac{R_C}{R_E}$$

A_i

$$A_i = -\frac{h_{fe} R_B}{R_B + Z_b}$$

or

$$A_i = -A_v \frac{Z_i}{R_C}$$

Emitter-follower Configuration(*common-collector* configuration **):**

- When the output is taken from the emitter terminal of the transistor as shown in figure, the network is referred to as an *emitter-follower.*
- The output voltage is always slightly less than the input signal due to the drop from base to emitter, but the approximation $A_v \cong 1$ is usually a good one.
- The fact that V_o "follows" the magnitude of V_i with an in-phase relationship accounts for the terminology emitter-follower.
- The most common emitter-follower configuration appears in Fig. In fact, because the collector is grounded for ac analysis, it is actually a ***common-collector*** **configuration**.
- The emitter-follower configuration is frequently used for impedance-matching purposes.
- It presents a high impedance at the input and a low impedance at the output, which is the direct opposite of the standard fixed-bias configuration. The resulting effect is much the same as that obtained with a transformer, where a load is matched to the source impedance for maximum power transfer through the system.

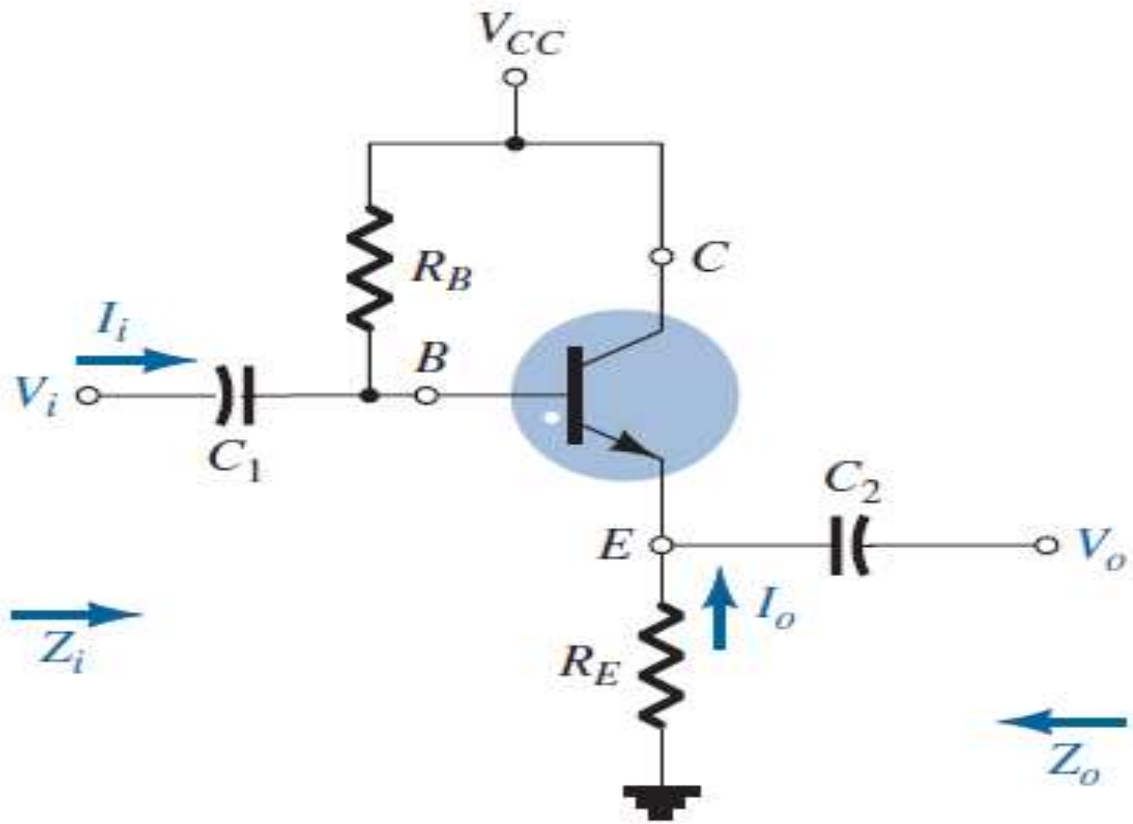


FIG.

Emitter-follower configuration.

Analysis of emitter follower using r_e model:

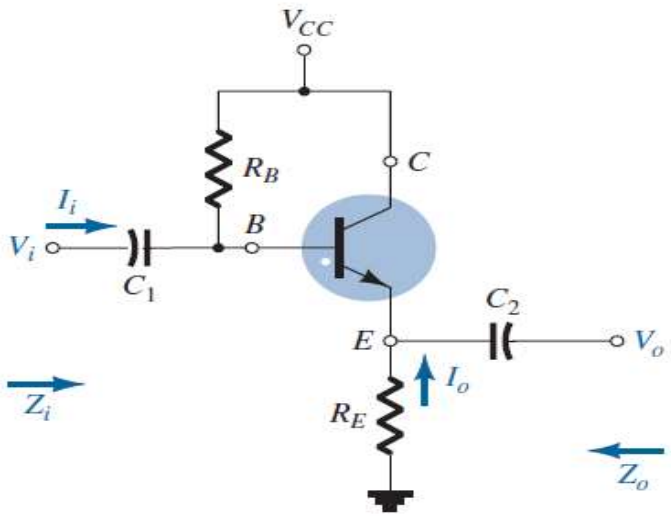


FIG.
Emitter-follower configuration.

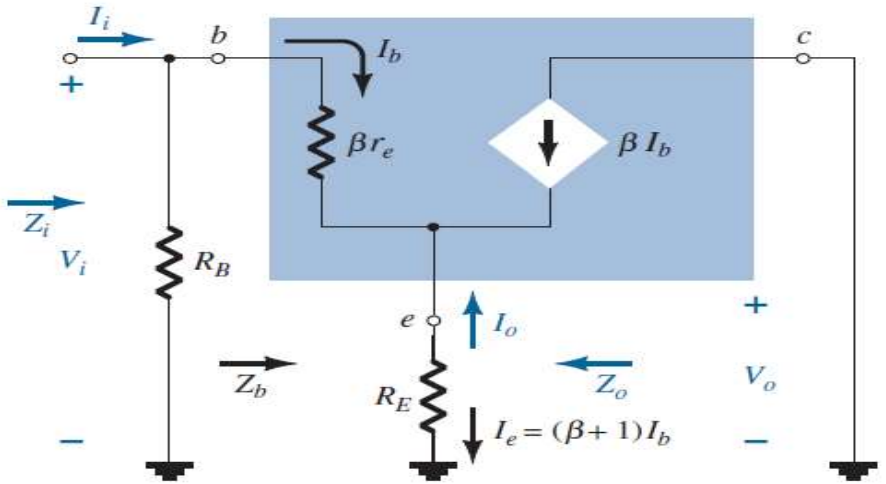


FIG.
Substituting the r_e equivalent circuit into the ac equivalent network of Fig.

Z_i The input impedance is determined in the same manner as described in the preceding section:

$$Z_i = R_B \| Z_b$$

with

$$Z_b = \beta r_e + (\beta + 1)R_E$$

or

$$Z_b \cong \beta(r_e + R_E)$$

and

$$Z_b \cong \beta R_E \qquad R_E \gg r_e$$

Z_o The output impedance is best described by first writing the equation for the current I_b,

$$I_b = \frac{V_i}{Z_b}$$

and then multiplying by $(\beta + 1)$ to establish I_e. That is,

$$I_e = (\beta + 1)I_b = (\beta + 1)\frac{V_i}{Z_b}$$

Substituting for Z_b gives

$$I_e = \frac{(\beta + 1)V_i}{\beta r_e + (\beta + 1)R_E}$$

or

$$I_e = \frac{V_i}{[\beta r_e/(\beta + 1)] + R_E}$$

but

$$(\beta + 1) \cong \beta$$

and

$$\frac{\beta r_e}{\beta + 1} \cong \frac{\beta r_e}{\beta} = r_e$$

so that

$$\boxed{I_e \cong \frac{V_i}{r_e + R_E}}$$

If we now construct the network defined by Eq. the configuration of Fig. results.

To determine Z_o, V_i is set to zero and

$$\boxed{Z_o = R_E \| r_e}$$

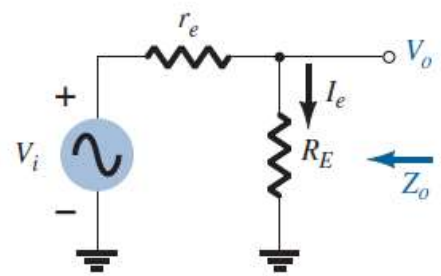


FIG.
Defining the output impedance for the emitter-follower configuration.

Because R_E is typically much greater than r_e, the following approximation is often applied:

$$\boxed{Z_o \cong r_e}$$

A_v Figure 38 can be used to determine the voltage gain through an application of the voltage-divider rule:

$$V_o = \frac{R_E V_i}{R_E + r_e}$$

and

$$\boxed{A_v = \frac{V_o}{V_i} = \frac{R_E}{R_E + r_e}}$$

Because R_E is usually much greater than r_e, $R_E + r_e \cong R_E$ and

$$\boxed{A_v = \frac{V_o}{V_i} \cong 1}$$

Analysis of Emitter-follower Configuration using Hybrid Model:

- For the emitter-follower, the small-signal ac model will be the same as r_e model analysis with $\beta r_e = h_{ie}$ and $\beta = h_{fe}$.
- The analysis will proceed in the same manner as r_e model analysis of emitter follower.

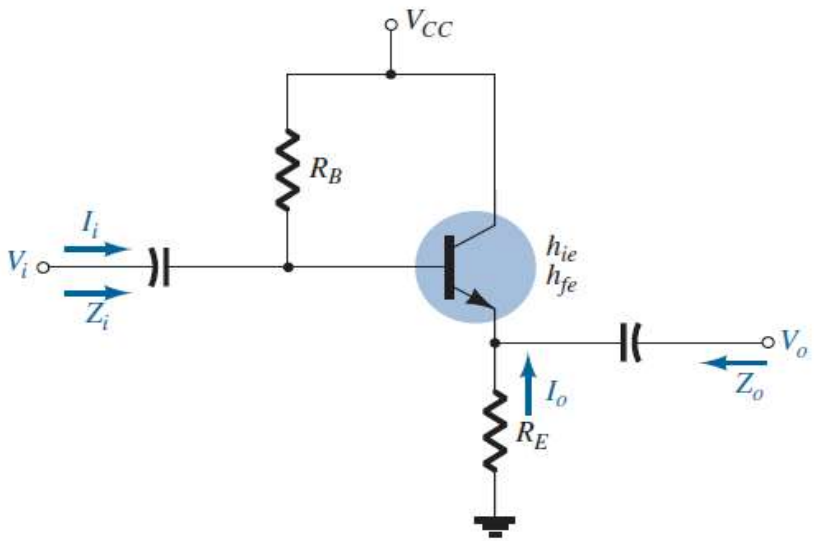


FIG.
Emitter-follower configuration.

Z_i

$$Z_b \cong h_{fe}R_E$$

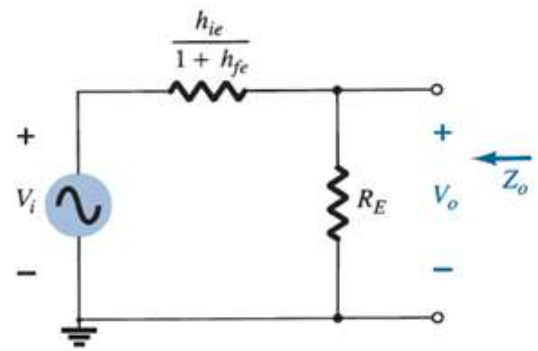
$$Z_i = R_B \| Z_b$$

Z_o For Z_o, the output network defined by the resulting equations will appear as shown in Fig.

$$Z_o = R_E \| \frac{h_{ie}}{1 + h_{fe}}$$

or, because $1 + h_{fe} \cong h_{fe}$,

$$Z_o \cong R_E \| \frac{h_{ie}}{h_{fe}}$$



Defining Z_o for the emitter-follower configuration.

A_v For the voltage gain, the voltage-divider rule can be applied

$$V_o = \frac{R_E(V_i)}{R_E + h_{ie}/(1 + h_{fe})}$$

but, since $1 + h_{fe} \cong h_{fe}$,

$$A_v = \frac{V_o}{V_i} \cong \frac{R_E}{R_E + h_{ie}/h_{fe}}$$

A_i

$$A_i = \frac{h_{fe} R_B}{R_B + Z_b}$$

or

$$A_i = -A_v \frac{Z_i}{R_E}$$

Contents of the Class:

- Cascaded Systems
- Cascode Connection
- **Darlington Connection**
- **Feedback pair**
- hybrid pi model
- **Junction Field Effect Transistors (JFETs)**

Cascaded Systems:

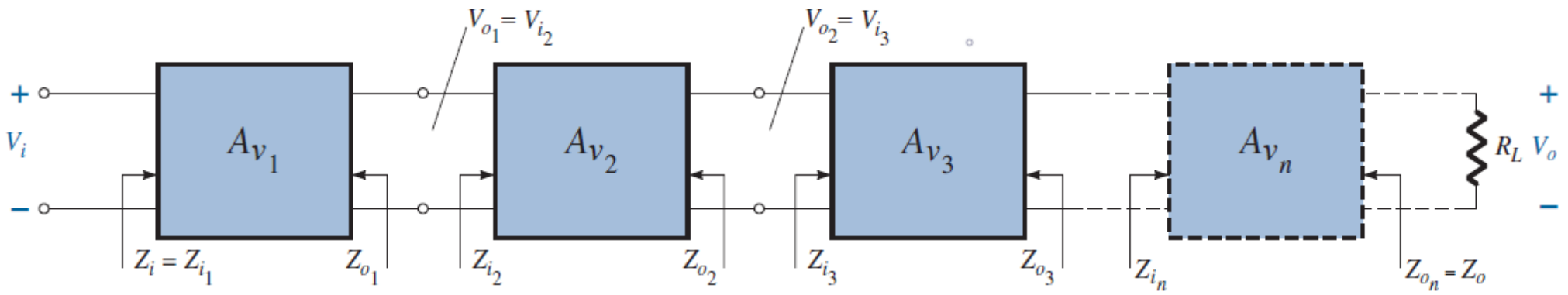


FIG.
Cascaded system.

Cascaded Systems:

- When two or more amplifier are cascaded such as that appearing

where $A_{v_1}, A_{v_2}, A_{v_3}$, and so on, are the voltage gains of each stage

under loaded conditions. That is, A_{v_1} is determined with the *input impedance to* A_{v_2} *acting as the load on* A_{v_1}. For A_{v_2}, A_{v_1} will determine the signal strength and source impedance at the input to A_{v_2}. The total gain of the system is then determined by the product of the individual gains as follows:

$$A_{v_T} = A_{v_1} \cdot A_{v_2} \cdot A_{v_3} \cdots$$

and the total current gain is given by

$$A_{i_T} = -A_{v_T} \frac{Z_{i_1}}{R_L}$$

RC-Coupled BJT Amplifiers:

- One popular connection of amplifier stages is the *RC*-coupled variety shown in Fig. The name is derived from the capacitive coupling capacitor *Cc* and the fact that the load on the first stage is an *RC* combination.
- The coupling capacitor isolates the two stages from a dc viewpoint but acts as a short-circuit equivalent for the ac response. The input impedance of the second stage acts as a load on the first

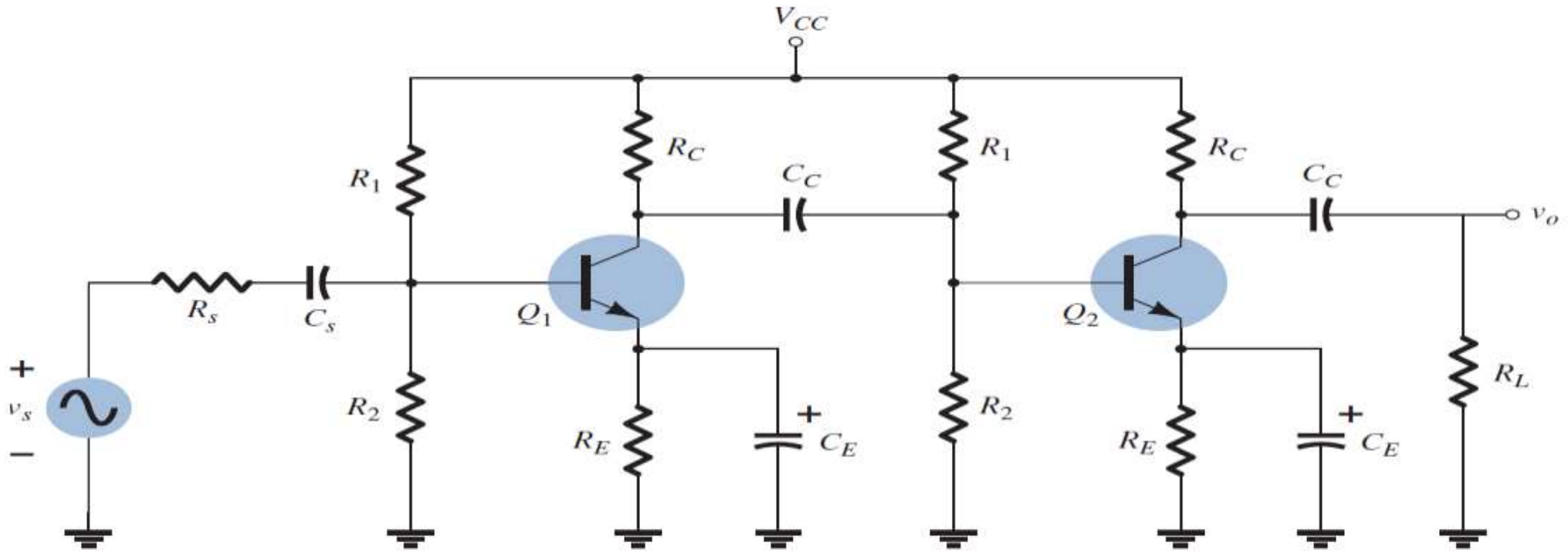


FIG.
R–C coupled BJT amplifiers.

Cascode Connection:

- The cascode configuration has two configurations. In each case the collector of the leading transistor is connected to the emitter of the following transistor.
- The arrangements provide a relatively high-input impedance with low voltage gain for the first stage to ensure the input Miller capacitance is at a minimum, whereas the following CB stage provides an excellent high-frequency response.

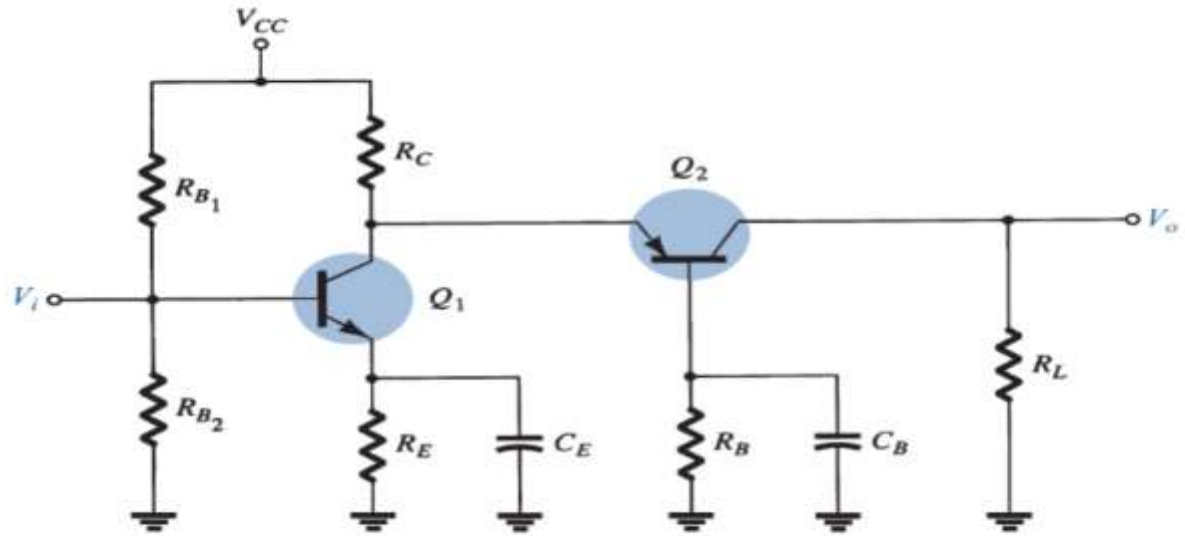


FIG.
Cascode configuration.

A Practical cascode Circuits:

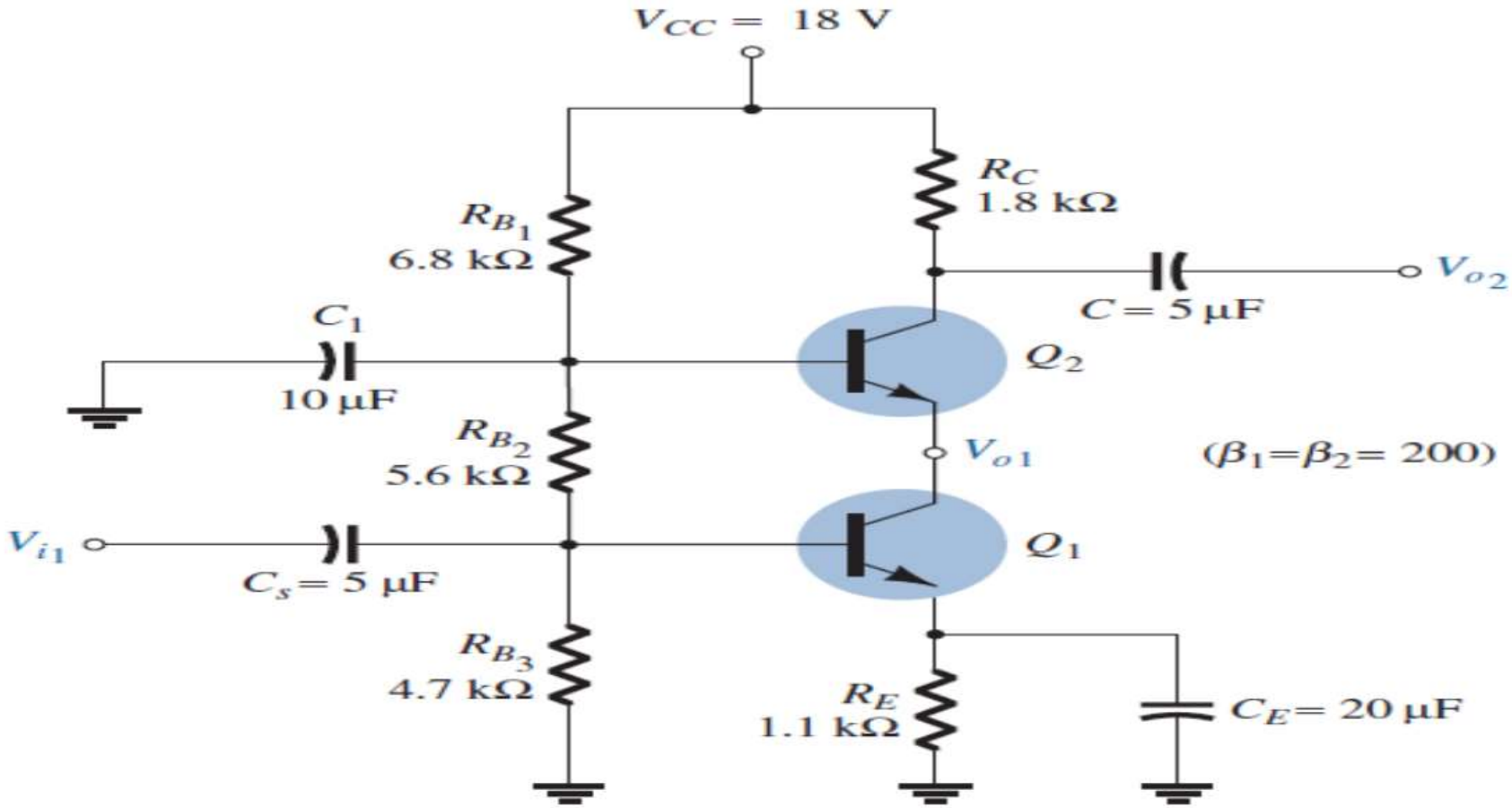


FIG.
Practical cascode circuit for Example 16.

Darlington Connection:

- A very popular connection of two bipolar junction transistors for operation as one "superbeta" transistor is the Darlington connection shown in Fig. The main feature of the Darlington connection is that the composite transistor acts as a single unit with a current gain that is the product of the current gains of the individual transistors. If the connection is made using two separate transistors having current gains of β_1 and β_2,

the Darlington connection provides a current gain of $\beta_D = \beta_1\beta_2$

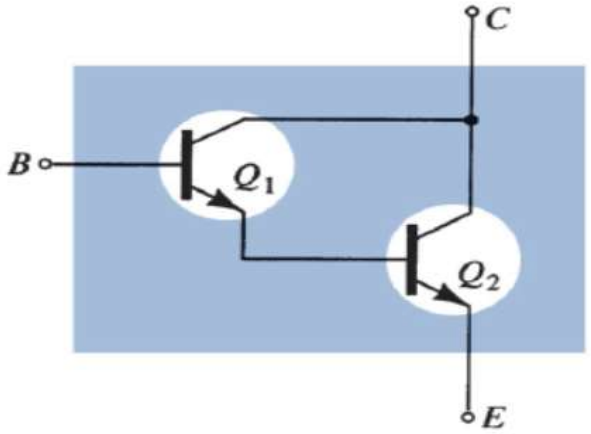


FIG.
Darlington combination.

Emitter-Follower Configuration with darlington amplifier:

- A Darlington amplifier used in an emitter-follower configuration appears in Fig. The primary impact of using the Darlington configuration is an input impedance much larger than that obtained with a single-transistor network. The current gain is also larger, but the voltage gain for a single-transistor or Darlington configuration remains slightly less than one.

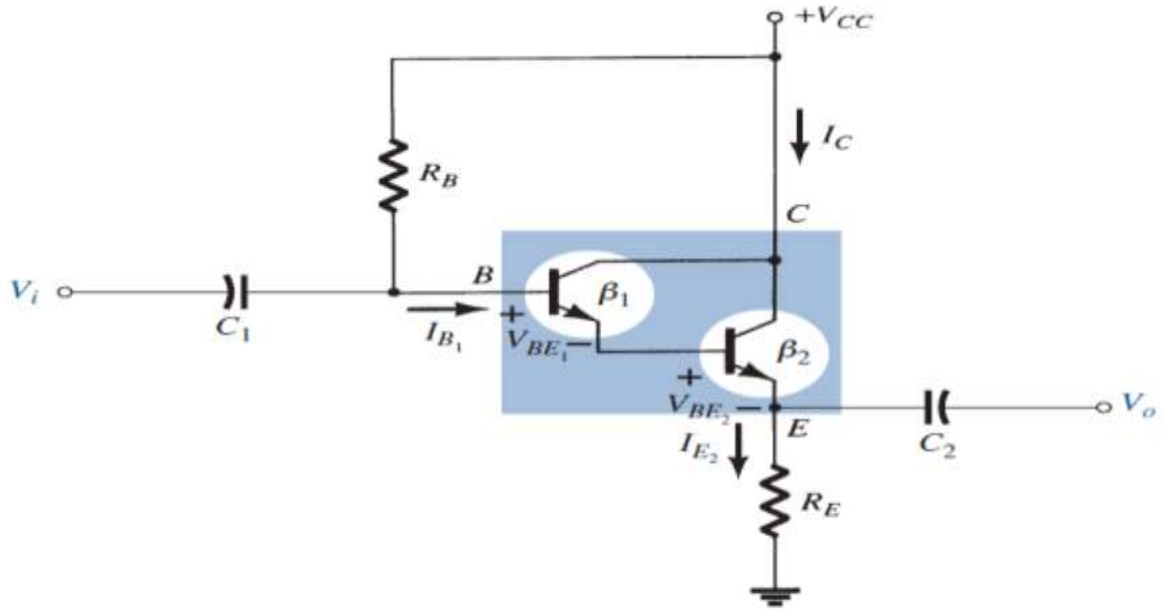


FIG.
Emitter-follower configuration with a Darlington amplifier.

Feedback pair:

- The feedback pair connection is a two-transistor circuit that operates like the Darlington circuit. Notice that the feedback pair uses a *pnp* transistor driving an *npn* transistor, the two devices acting effectively much like one *pnp* transistor. As with a Darlington connection, the feedback pair provides very high current gain (the product of the transistor current gains), high input impedance, low output impedance, and a voltage gain slightly less than one. Initially, it may appear that it would have a high voltage gain because the output is taken off the collector with a resistor *RC* in place. However, the *pnp*–*npn* combination results in terminal characteristics very similar to that of the emitter–follower configuration. A typical application uses a Darlington and a feedback-pair connection to provide complementary transistor operation.

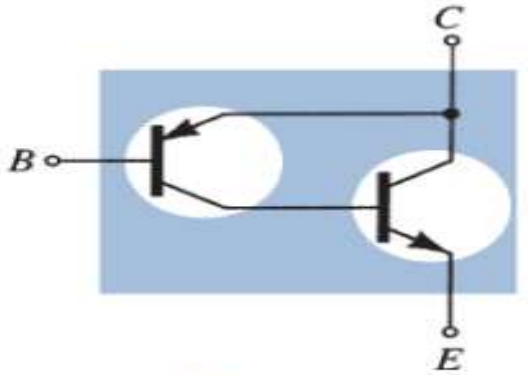


FIG.
Feedback pair connection.

HYBRID π MODEL

- The last transistor model to be introduced is the hybrid pi model of Fig. which includes parameters that do not appear in the other two models primarily to provide a more accurate model for high-frequency effects.

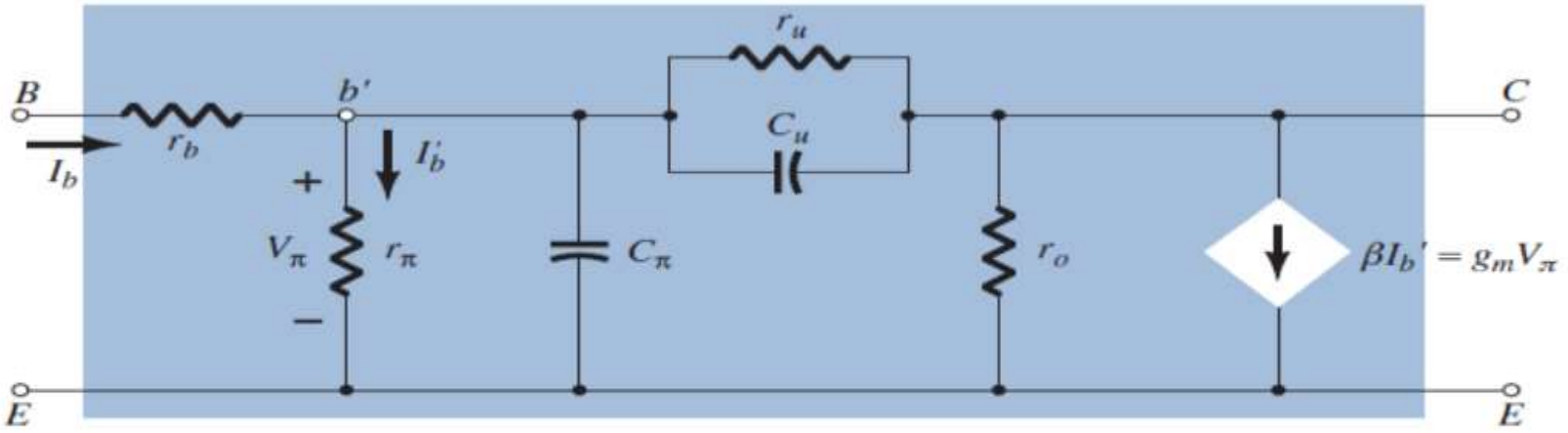


FIG.

Giacoletto (or hybrid π) high-frequency transistor small-signal ac equivalent circuit.

r_π, r_o, r_b, and r_u

The resistors r_π, r_o, r_b, and r_u are the resistances between the indicated terminals of the device when the device is in the active region. The resistance r_π (using the symbol π to agree with the hybrid π terminology) is simply βr_e as introduced for the common-emitter r_e model.

That is,

$$r_\pi = \beta r_e$$

The output resistance r_o is the output resistance normally appearing across an applied load. Its value, which typically lies between 5 kΩ and 40 kΩ, is determined from the hybrid parameter h_{oe}, the Early voltage, or the output characteristics.

The resistance r_b includes the base contact, base bulk, and base spreading resistance levels. The first is due to the actual connection to the base. The second includes the resistance from the external terminal to the active region of the transistor, and the last is the actual resistance within the active base region. It is typically a few ohms to tens of ohms.

The resistance r_u (the subscript u refers to the *union* it provides between collector and base terminals) is a very large resistance and provides a feedback path from output to input circuits in the equivalent model. It is typically larger than βr_o, which places it in the megohm range.

C_π and C_u

All the capacitors that appear in Fig. are stray parasitic capacitors between the various junctions of the device. They are all capacitive effects that really only come into play at high frequencies. For low to mid-frequencies their reactance is very large, and they can be considered open circuits. The capacitor C_π across the input terminals can range from a few pF to tens of pF. The capacitor C_u from base to collector is usually limited to a few pF but is magnified at the input and output by an effect called the Miller effect.

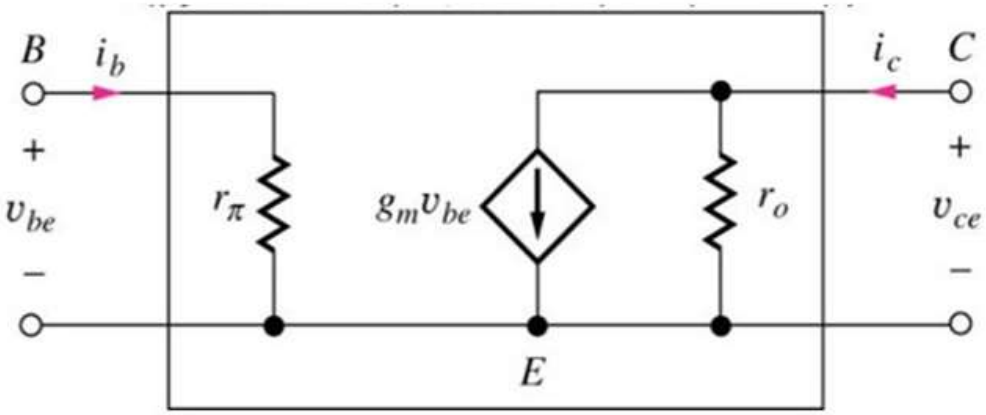
$\beta I_b'$ or $g_m V_\pi$

It is important to note in Fig. that the controlled source can be a voltage-controlled current source (VCCS) or a current-controlled current source (CCCS), depending on the parameters employed.

$$g_m = \frac{1}{r_e}$$

$$r_o = \frac{1}{h_{oe}}$$

Hybrid-Pi Model for Low frequency representation of BJT:



- The hybrid-pi small-signal model is the intrinsic low-frequency representation of the BJT.
- The small-signal parameters are control led by the Q-point and are independent of the geometry of the BJT.

Transconductance:

$$g_m = \frac{I_C}{V_T}, V_T = \frac{KT}{q}$$

Input resistance: Rin

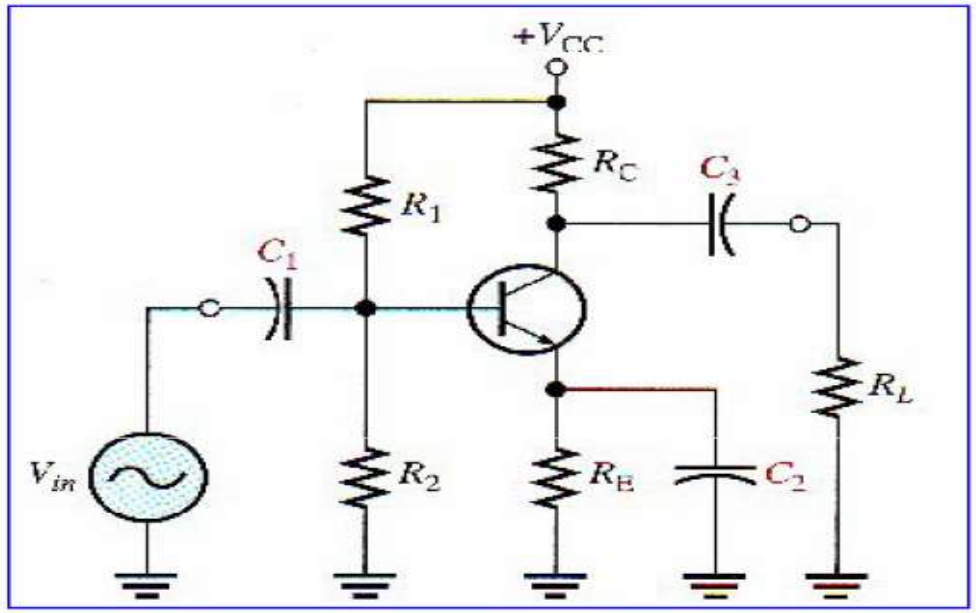
$$r_\pi = \frac{\beta_o V_T}{I_C} = \frac{\beta_o}{g_m}$$

Output resistance:

$$r_o = \frac{V_A + V_{CE}}{I_C}$$

Where, V_A is Early Voltage (V_A=100V for npn)

Frequency Response of CE BJT Amplifier



$$X_C = \frac{1}{2\pi \times f \times C}$$

Assuming that the coupling and bypass capacitors are ideal shorts at the midrange signal frequency, the midrange voltage gain can be determined by

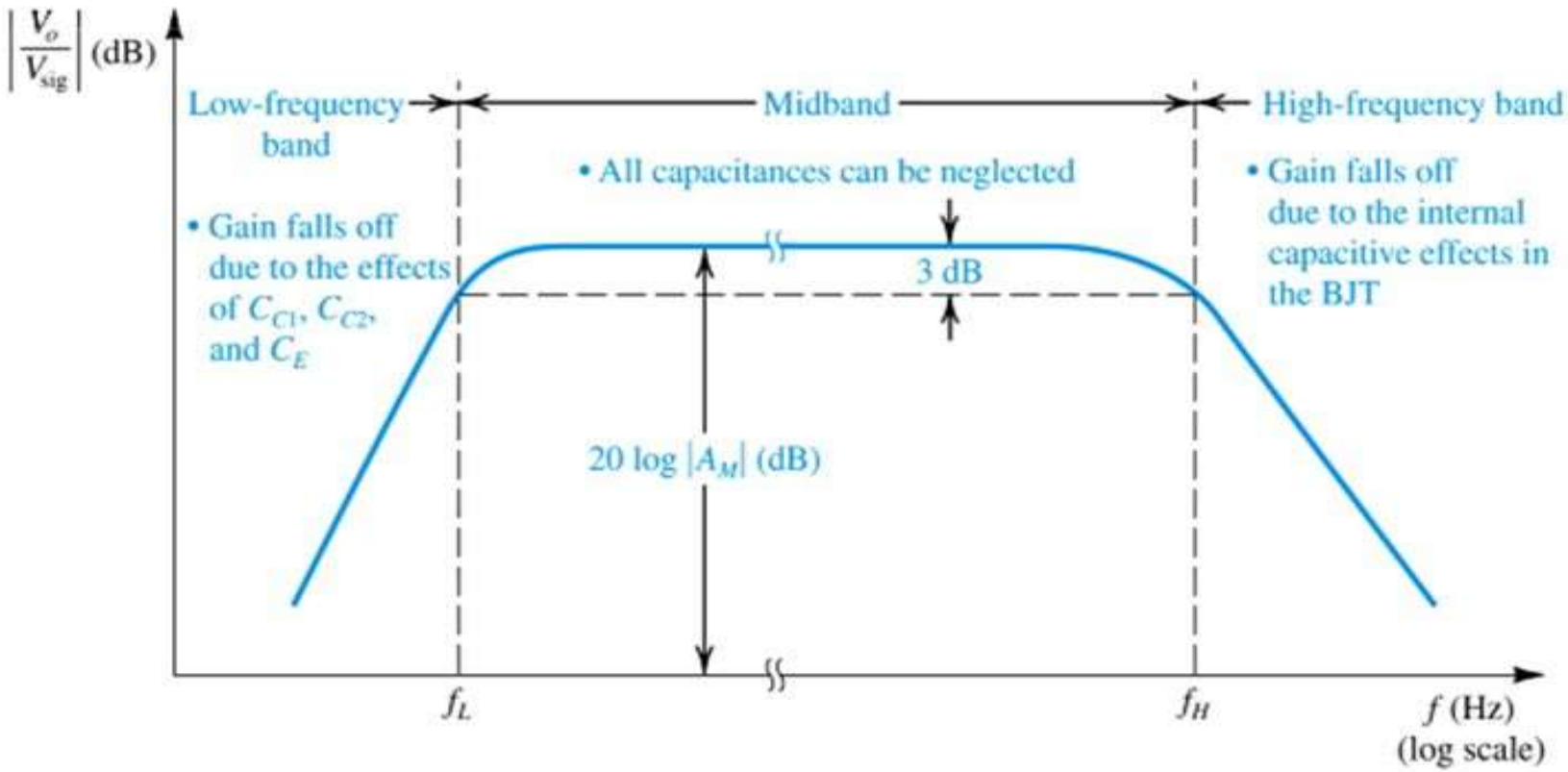
$$A_{v,mid} = \frac{(R_C \backslash\backslash R_L)}{r_e'}$$

- In the low frequency range, BJT amplifier *has three high-pass RC circuits, namely input, bypass and output RC circuit, that affect its gain.*

- The lower cutoff frequency of a given common emitter amplifier will be given by the highest of the individual RC circuits.

$$f_{C\text{-}low} = MAX(f_{c\text{-}input}, f_{c\text{-}output}, f_{c\text{-}bypass})$$

Typical Frequency response



Effects of Frequency on Operation of Circuits

- Increase in the ***number of stages*** could also affect the frequency response of a circuit.
- In general, the ***gain*** of amplifier circuits ***decreases at low and high frequencies***.
- The ***cutoff frequencies*** are the frequencies when the power delivered to the load of the circuit becomes ***half the power*** delivered to the load at middle frequencies.

Av_{mid} = voltage gain of amplifier at middle frequencies
0.707 Av_{mid} = voltage gain of amplifier at lower cutoff frequency and higher cutoff frequency (when output power is half the output power at middle frequencies)
f1 = low cutoff frequency $P_{O(HPF)}$ = output power at higher cutoff frequency Vi = input voltage
f2 = high cutoff frequency $P_{O(LPF)}$ = output power at lower cutoff frequency
Pomid = output power at middle frequencies

$$P_{O(HPF)} = P_{O(LPF)} = \frac{(0.707 A_{vmid}\, Vi)^2}{Ro} = 0.5 \frac{(A_{vmid}\, Vi)^2}{Ro} = 0.5\, P_{Omid}$$

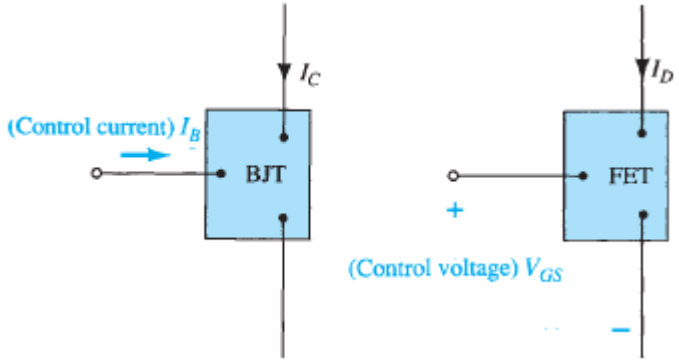
Field Effect Transistors (FETs):

- Field effect transistors are unipolar device because current is carried by only one type of carriers (majority carriers) while BJTs were bipolar.
- FETs are voltage controlled device where output current is controlled by voltage between two terminals gate and source while BJTs were current controlled device.

FETs are characterized by very high input resistance (in mega ohm) while BJT have high gain.

FETs are less sensitive to temperature variations and are more easily integrated on ICs.

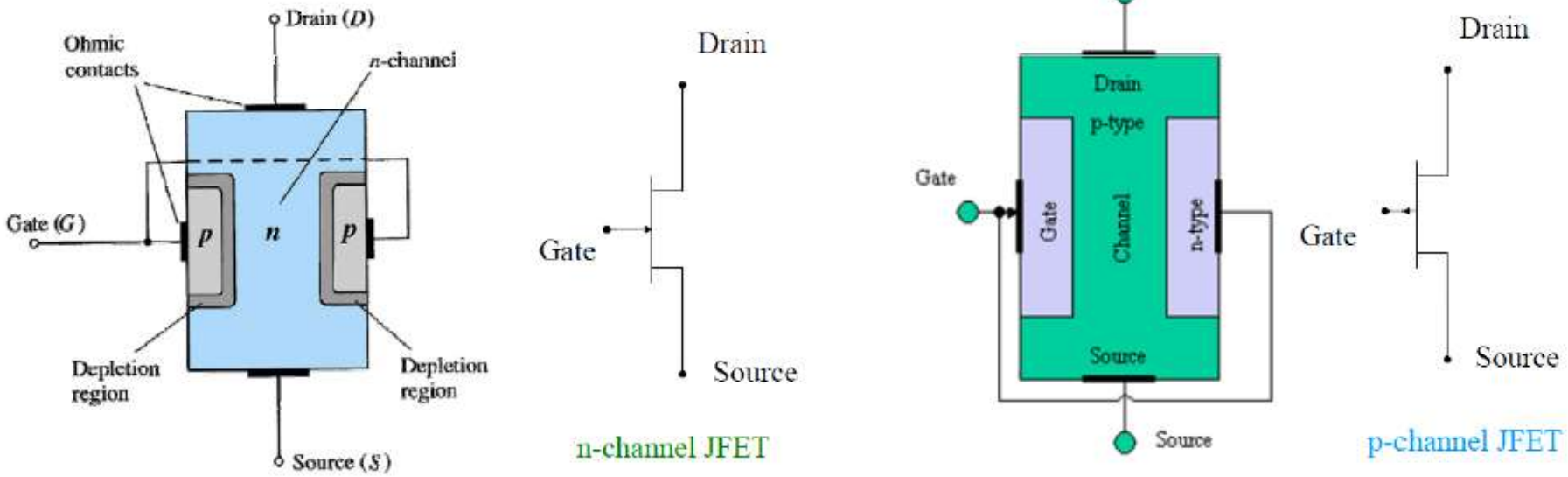
Types of FETs:
Junction Field Effect Transistor (JFET)
Metal Oxide semiconductor Field Effect Transistor (MOSFET)



$$I_C = \beta I_B \qquad I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Junction Field Effect Transistors (JFETs):

- Junction field effect transistor (JFET) is a type FET that operates with a reverse biased p-n junction to control current in a channel.
- Depending on the structure, JFET fall in two categories: n channel and p channel JFET



Operation of n channel FET:

JFET at V_{GS}=0 and V_{DS} > 0

- JFET has two p-n junction. When V_{GS}=0 , both gate and source are at same potential so depletion region in low end of each p material is similar.
- The depletion region is wider near the top of both p type material because of higher potential at upper region. (Upper end of n-channel (drain) is at V_D and lower end (source) is at ground)
- The instant V_{DS} is applied across the channel, the electrons are drawn towards the drain giving drain current.
- As the V_{DS} is increased from 0V to a few V, the current

will increase according to Ohm's law.

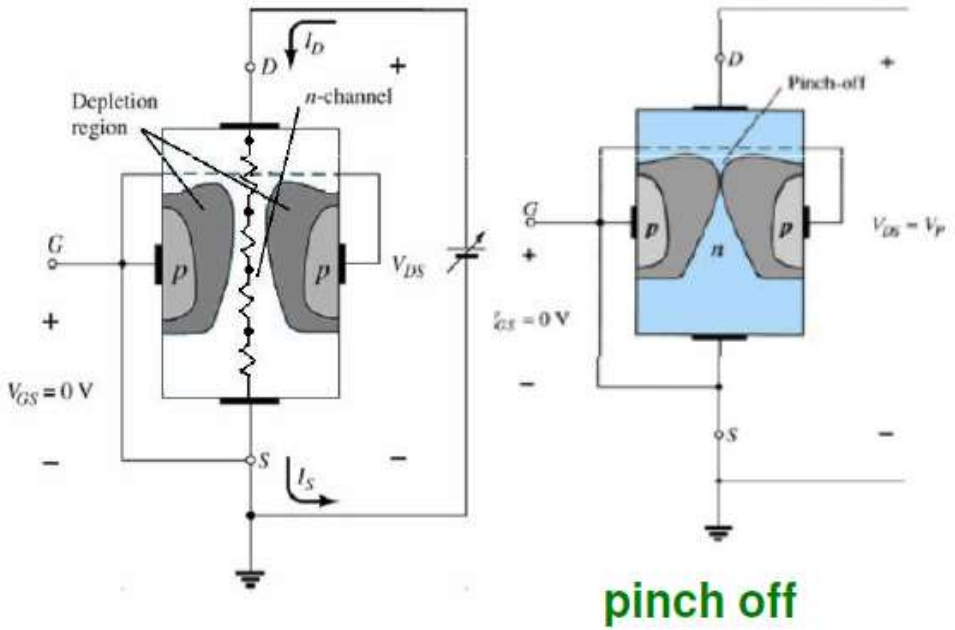
- As the V_{DS} approaches to Vp, the depletion width

increases causing a reduction in channel width.

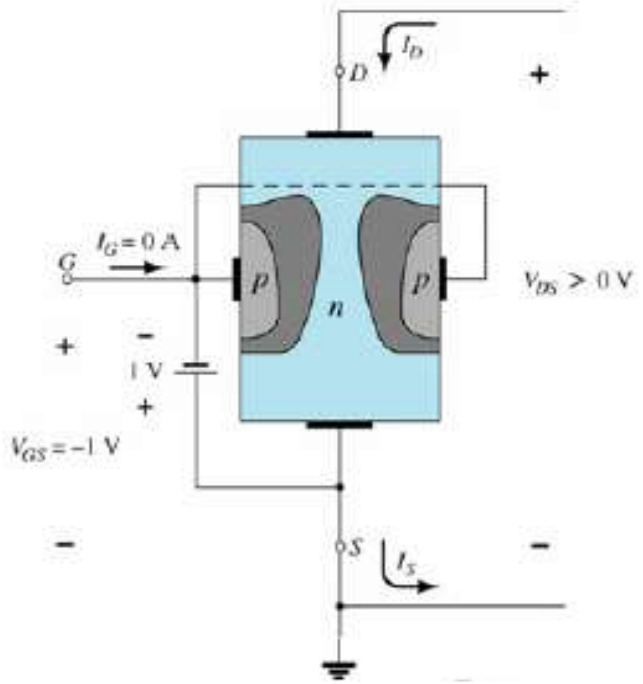
- **The value of V_{DS}** (at **V_{GS}=0) for which two**

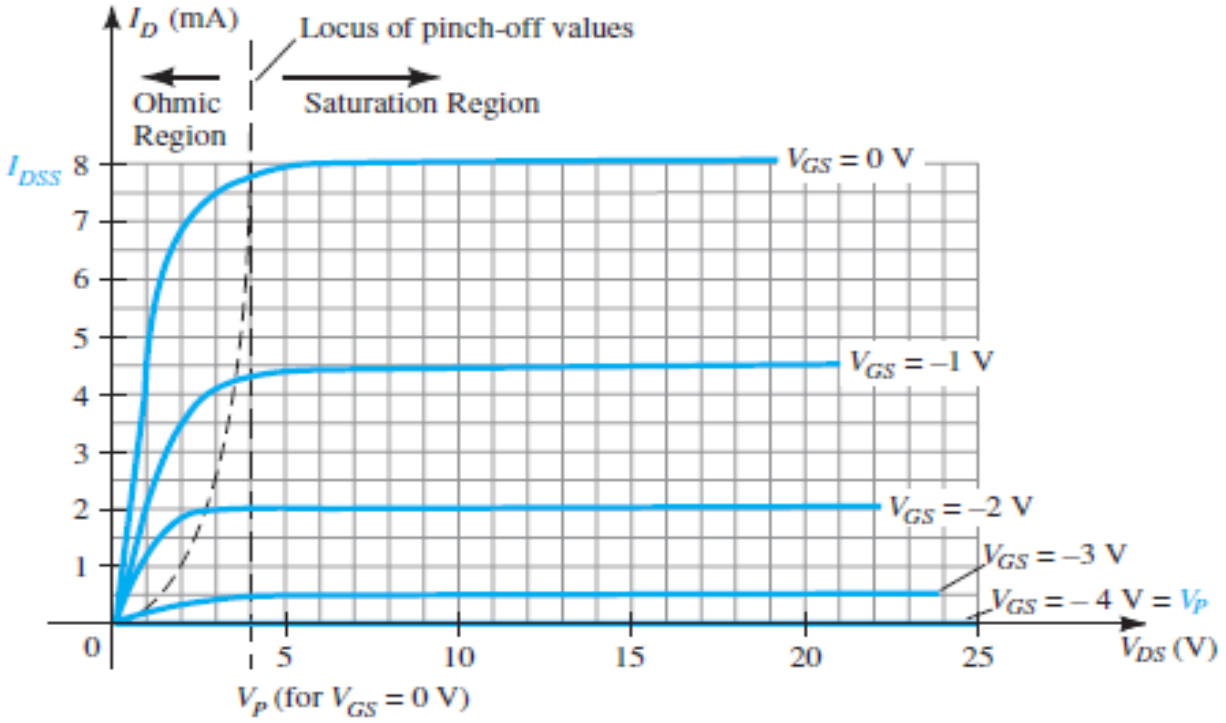
depletion region touches is called pinch off voltage

and denoted by V_P .



JFET at $V_{GS} < 0$ and $V_{DS} > 0$





The level of V_{GS} that results in $I_D = 0$ mA is $V_{GS} = V_P$

Vp is a negative voltage for n-channel and positive for p-channel JFETs.

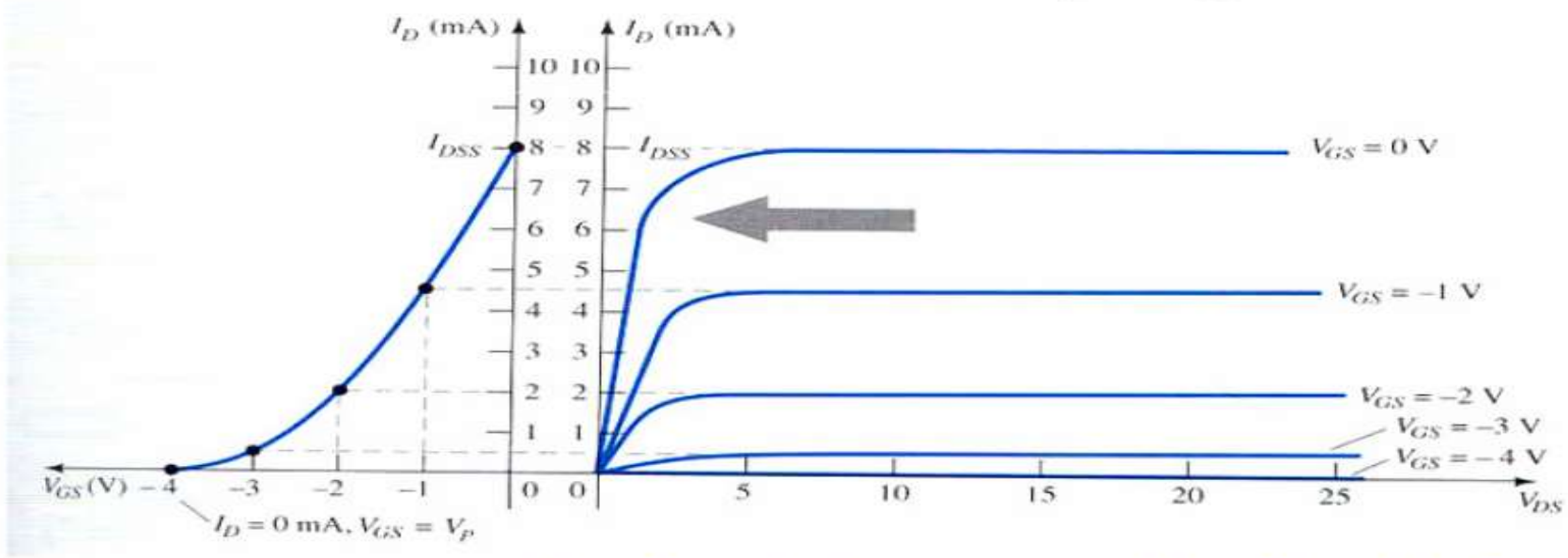
Transfer Characteristics

The relationship between I_D and V_{GS} is defined by Shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Where I_{DSS} and V_P are constants and V_{GS} is variable and controllable

The transfer function curve may be plotted from the characteristic curve, as shown. Notice the parabolic shape due to the square term relationship between I_D and V_{GS}



Remember that, when $V_{GS} = 0$, $I_D = I_{DSS}$ and when $V_{GS} = V_P$, $I_D = 0$ mA

Contents of the Class:

- Biasing of the JFET

1)FET in fixed bias

2)Self-bias

3)Voltage Divider Biasing

- From book- R. L. Boylestad

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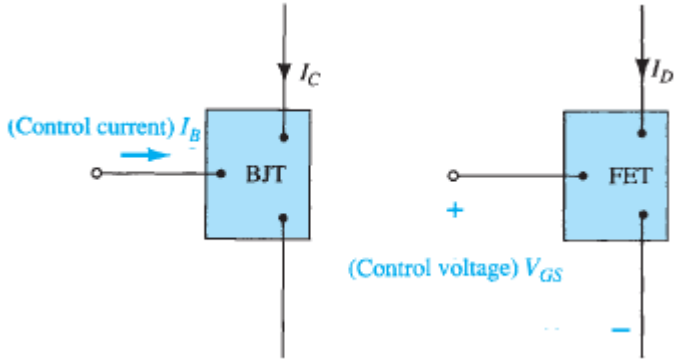

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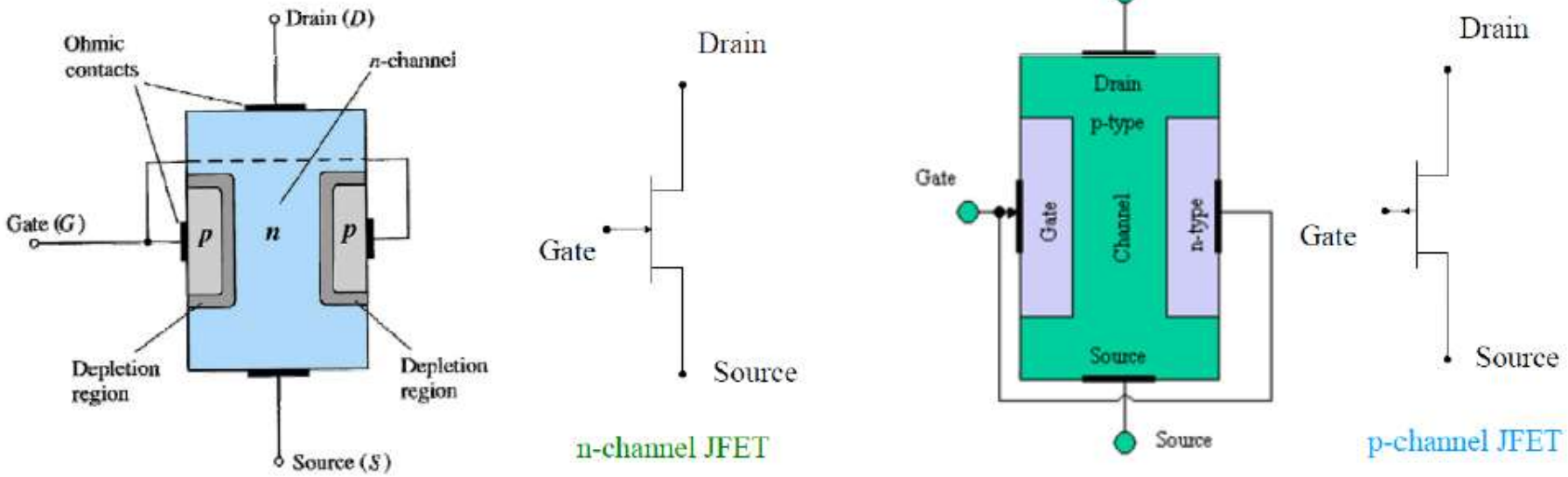

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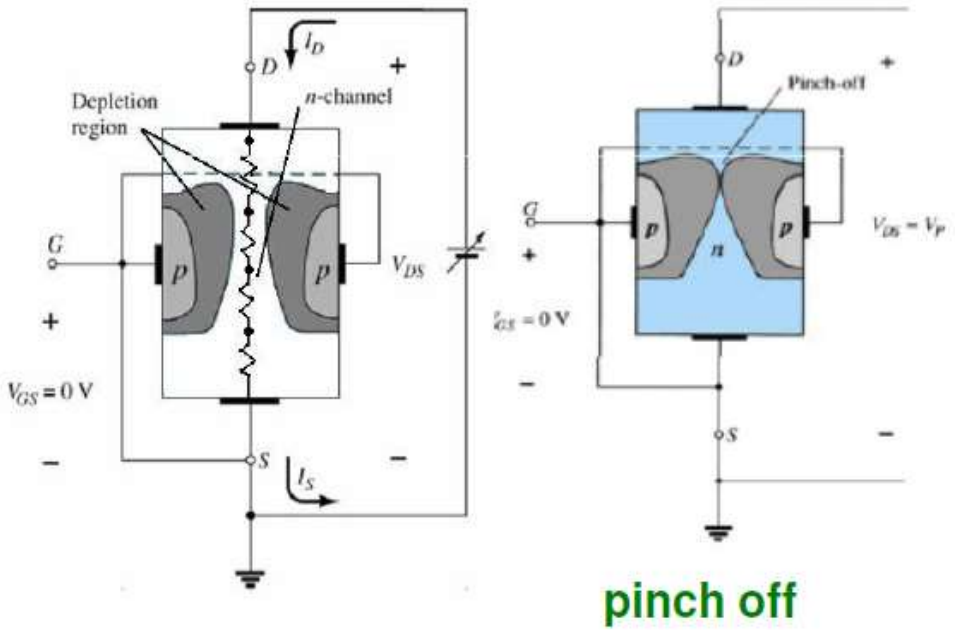
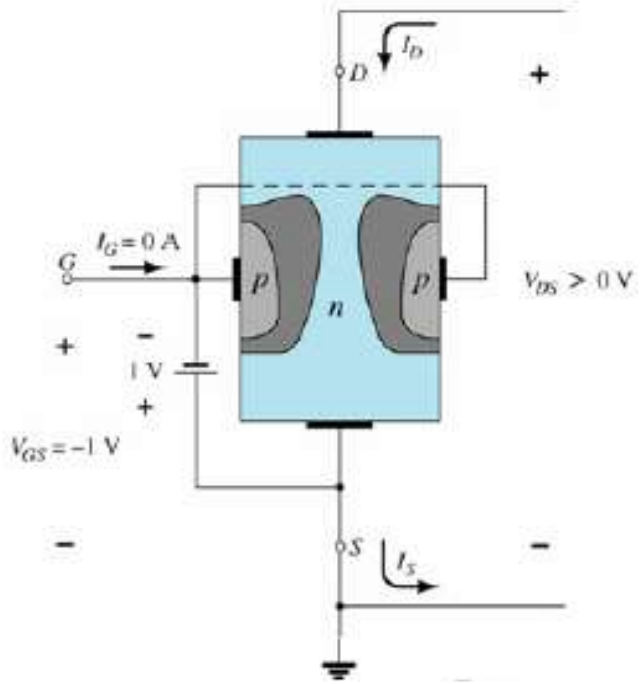
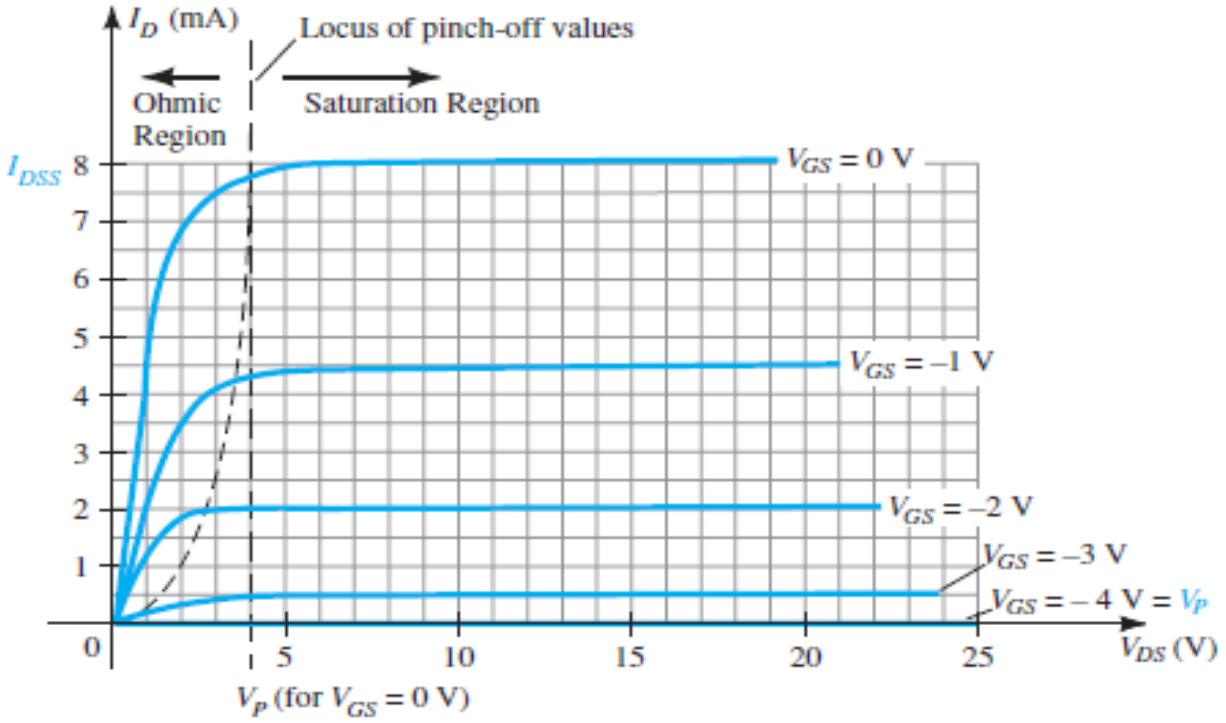


JFET at $V_{GS} < 0$ and $V_{DS} > 0$





The level of V_{GS} that results in $I_D = 0$ mA is $V_{GS} = V_P$

Vp is a negative voltage for n-channel and positive for p-channel JFETs.

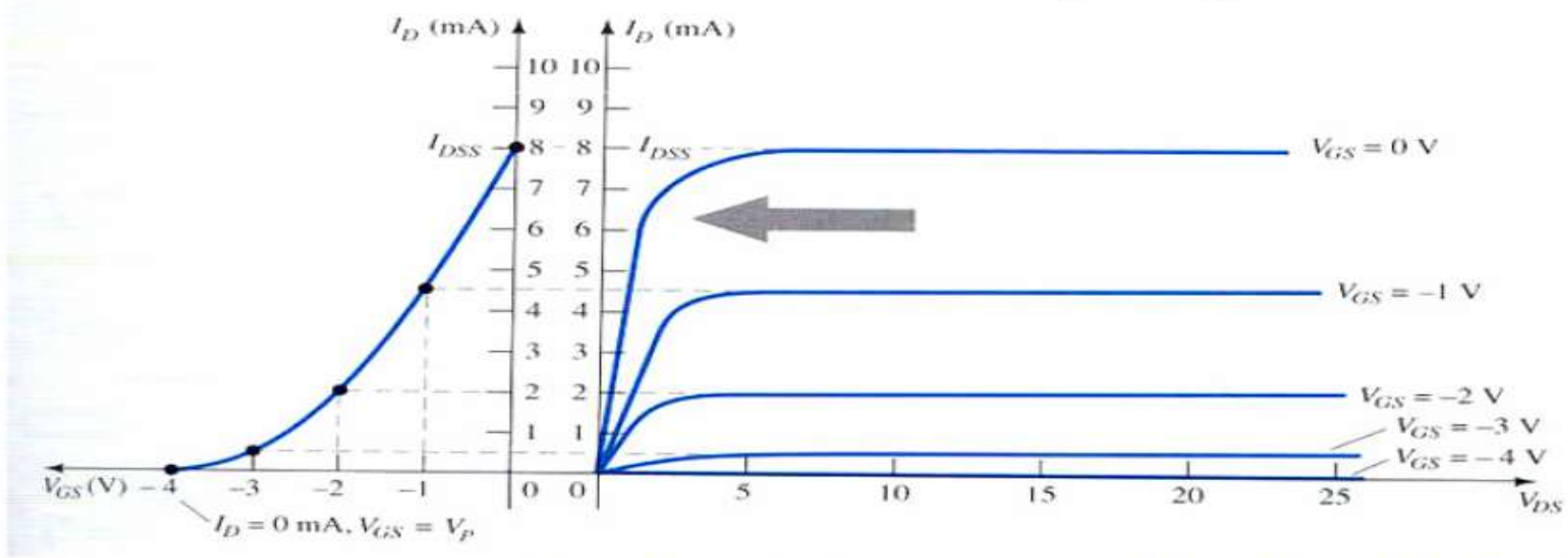
Transfer Characteristics

The relationship between I_D and V_{GS} is defined by Shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Where I_{DSS} and V_P are constants and V_{GS} is variable and controllable

The transfer function curve may be plotted from the characteristic curve, as shown. Notice the parabolic shape due to the square term relationship between I_D and V_{GS}

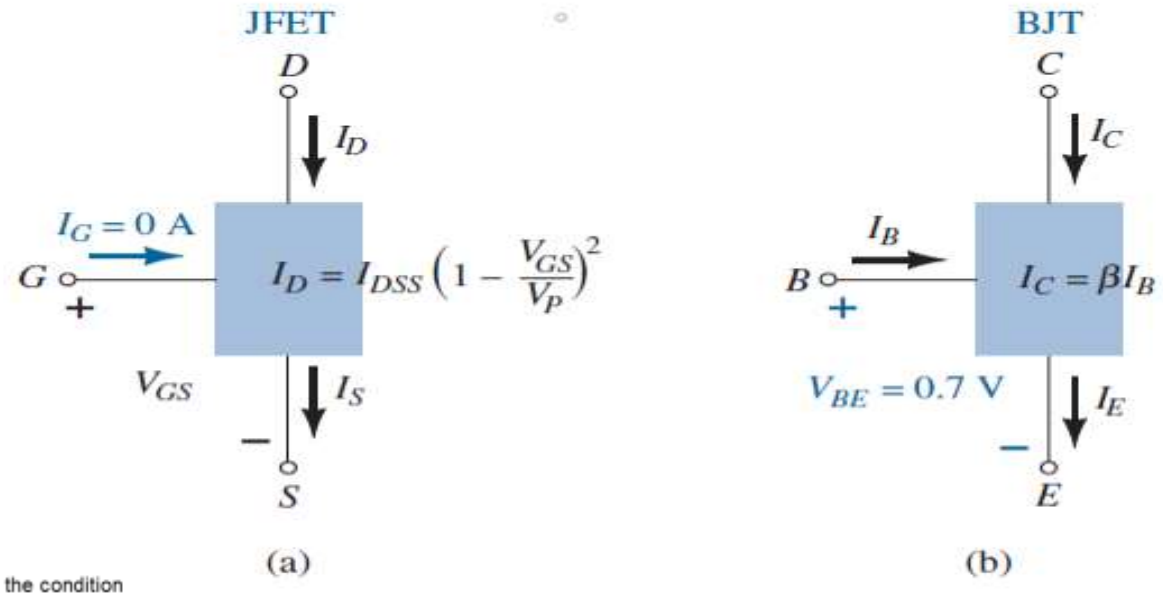


Remember that, when $V_{GS} = 0$, $I_D = I_{DSS}$ and when $V_{GS} = V_P$, $I_D = 0$ mA

Important Relationship:

A number of important equations and operating characteristics for the JFET have been introduced that are of particular importance for the analysis of dc and ac configurations that will follow.

JFET		BJT
$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	$\Leftrightarrow$	$I_C = \beta I_B$
$I_D = I_S$	$\Leftrightarrow$	$I_C \cong I_E$
$I_G \cong 0\ \text{A}$	$\Leftrightarrow$	$V_{BE} \cong 0.7\ \text{V}$



Recall that $V_{BE} = 0.7$ V was often the key to initiating an analysis of a BJT configuration. Similarly, the condition $I_G = 0$ A is often the starting point for the analysis of a JFET configuration. For the BJT configuration, I_B is normally the first parameter to be determined. For the JFET, it is normally V_{GS}.

FIG.
(a) JFET versus (b) BJT.

FET Biasing:

- For the field-effect transistor, the relationship between input and output quantities is *nonlinear* due to the squared term in Shockley's equation. Linear relationships result in straight lines when plotted on a graph of one variable versus the other, whereas nonlinear functions result in curves as obtained for the transfer characteristics of a JFET. The nonlinear relationship between I_D and V_{GS} can complicate the **mathematical approach** to the dc analysis of FET configurations.
- A **graphical approach** may limit solutions to tenths-place accuracy, but it is a quicker method for most FET amplifiers.

The general relationships that can be applied to the dc analysis of all FET amplifiers are

$$I_G \cong 0\ \text{A}$$

and

$$I_D = I_S$$

For JFETs and depletion-type MOSFETs and MESFETs, Shockley's equation is applied to relate the input and output quantities:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

For enhancement-type MOSFETs and MESFETs, the following equation is applicable:

$$I_D = k(V_{GS} - V_T)^2$$

Fixed-Bias Configuration:

The simplest of biasing arrangements for the *n*-channel JFET appears FET configurations that can be solved just as directly using either a **mathematical or a graphical approach**. The coupling capacitors are "open circuits" for the dc analysis and low impedances (essentially short circuits) for the ac analysis.

The resistor R_G is present to ensure that V_i appears at the input to the FET amplifier for the ac analysis. For the dc analysis.

$$I_G \cong 0\ \text{A}$$

$$V_{R_G} = I_G R_G = (0\ \text{A})R_G = 0\ \text{V}$$

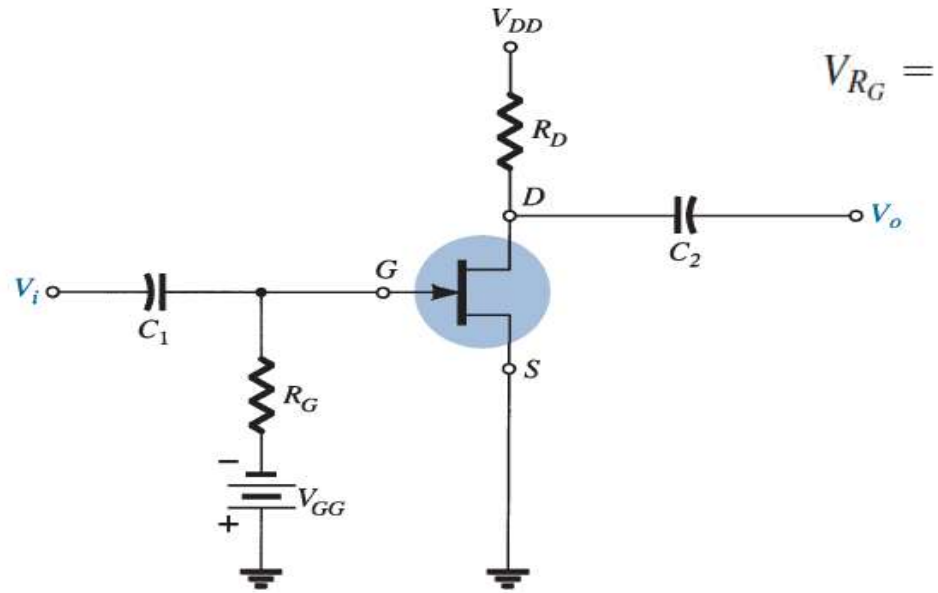


FIG.
Fixed-bias configuration.

Fixed-Bias Configuration:

- The zero-volt drop across R_G permits replacing R_G by a short-circuit equivalent, as appearing in the network of specifically redrawn for the dc analysis.

Applying Kirchhoff's voltage law in the clockwise direction of the indicated loop

$$-V_{GG} - V_{GS} = 0$$

$$\boxed{V_{GS} = -V_{GG}}$$

Since V_{GG} is a fixed dc supply, the voltage V_{GS} is fixed in magnitude, resulting in the designation "fixed-bias configuration."

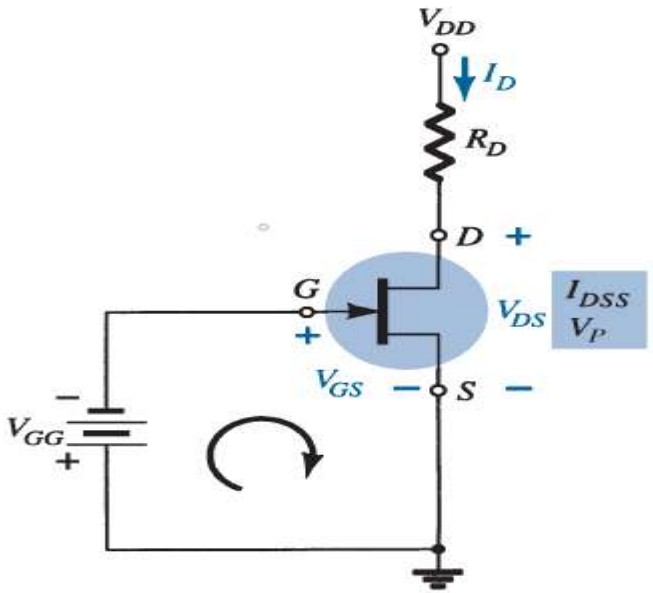


FIG.
Network for dc analysis.

The resulting level of drain current I_D is now controlled by Shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Since V_{GS} is a fixed quantity for this configuration, its magnitude and sign can simply be substituted into Shockley's equation and the resulting level of I_D calculated.

A graphical analysis

A graphical analysis would require a plot of Shockley's equation as shown in Fig.

Recall that choosing $V_{GS} = V_P/2$ will result in a drain current of $I_{DSS}/4$ when plotting the equation. For the analysis of this chapter, the three points defined by I_{DSS}, V_P, and the intersection just described will be sufficient for plotting the curve.

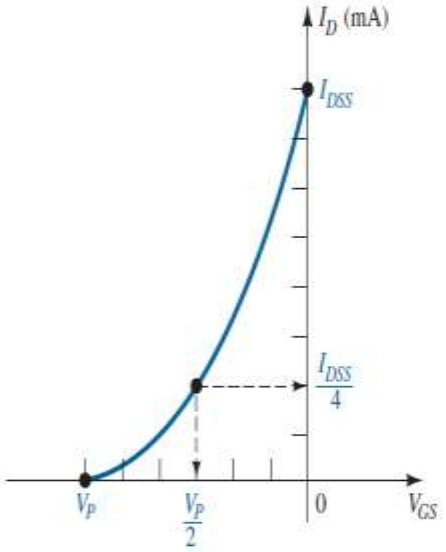


FIG.
Plotting Shockley's equation.

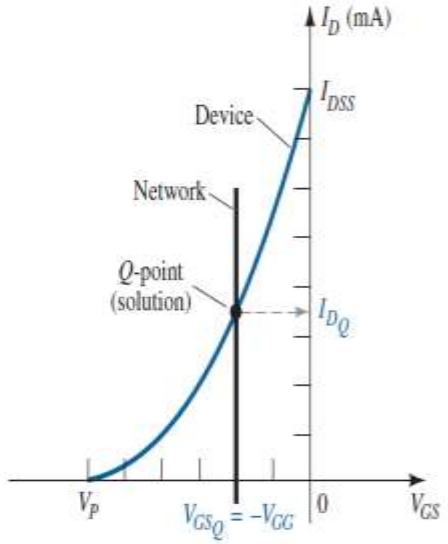


FIG.
Finding the solution for the fixed-bias configuration.

In Fig. the fixed level of V_{GS} has been superimposed as a vertical line at $V_{GS} = -V_{GG}$. At any point on the vertical line, the level of V_{GS} is $-V_{GG}$—the level of I_D must simply be determined on this vertical line. The point where the two curves intersect is the common solution to the configuration—commonly referred to as the *quiescent* or *operating point.* The subscript *Q* will be applied to the drain current and gate-to-source voltage to identify their levels at the *Q*-point. Note in Fig. that the quiescent level of I_D is determined by drawing a horizontal line from the *Q*-point to the vertical I_D axis.

The drain-to-source voltage of the output section can be determined by applying Kirchhoff's voltage law as follows:

$$+V_{DS} + I_D R_D - V_{DD} = 0$$

and

$$\boxed{V_{DS} = V_{DD} - I_D R_D}$$

Recall that single-subscript voltages refer to the voltage at a point with respect to ground.

$$\boxed{V_S = 0\text{ V}}$$

Using double-subscript notation, we have

$$V_{DS} = V_D - V_S$$

or

$$V_D = V_{DS} + V_S = V_{DS} + 0\text{ V}$$

and

$$\boxed{V_D = V_{DS}}$$

In addition,

$$V_{GS} = V_G - V_S$$

or

$$V_G = V_{GS} + V_S = V_{GS} + 0\text{ V}$$

and

$$\boxed{V_G = V_{GS}}$$

The fact that $V_D = V_{DS}$ and $V_G = V_{GS}$ is fairly obvious from the fact that $V_S = 0$ V, but the derivations above were included to emphasize the relationship that exists between double-subscript and single-subscript notation. Since the configuration requires two dc supplies, its use is limited and will not be included in the forthcoming list of the most common FET configurations.

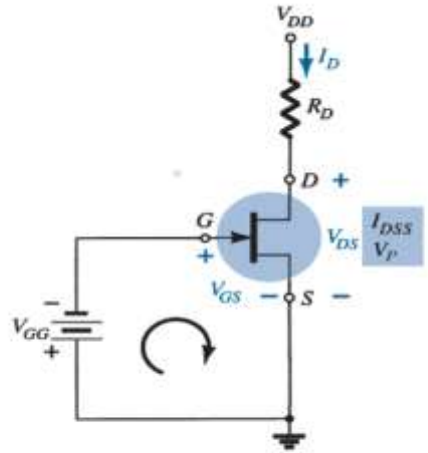


FIG.
Network for dc analysis.

EXAMPLE 1 Determine the following for the network of Fig.

a. V_{GS_Q}.
b. I_{D_Q}.
c. V_{DS}.
d. V_D.
e. V_G.
f. V_S.

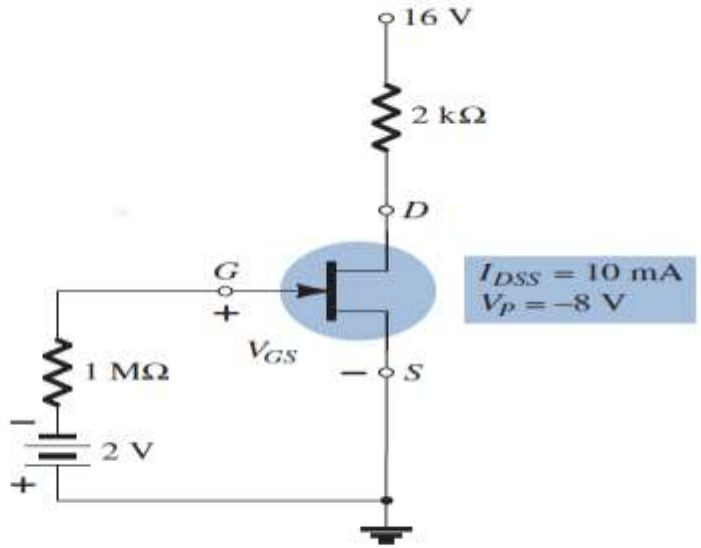


FIG.
Example 1.

Solution:

Mathematical Approach

a. $V_{GS_Q} = -V_{GG} = \mathbf{-2\ V}$

b. $$I_{D_Q} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10\text{ mA}\left(1 - \frac{-2\text{ V}}{-8\text{ V}}\right)^2$$
$$= 10\text{ mA}(1 - 0.25)^2 = 10\text{ mA}(0.75)^2 = 10\text{ mA}(0.5625)$$
$$= \mathbf{5.625\ mA}$$

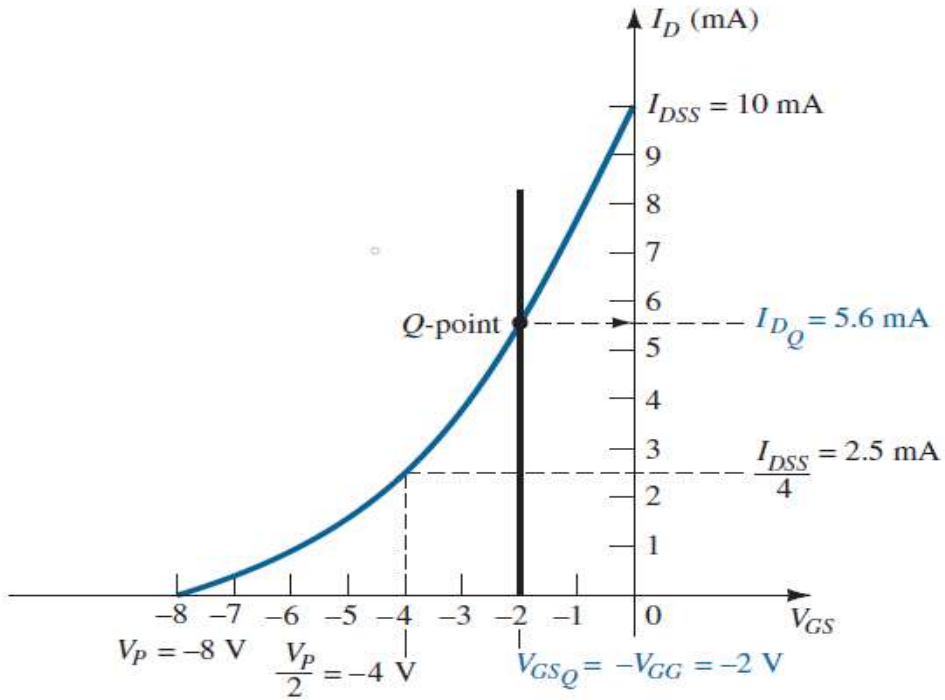
c. $$V_{DS} = V_{DD} - I_D R_D = 16\text{ V} - (5.625\text{ mA})(2\text{ k}\Omega)$$
$$= 16\text{ V} - 11.25\text{ V} = \mathbf{4.75\ V}$$

d. $V_D = V_{DS} = \mathbf{4.75\ V}$

e. $V_G = V_{GS} = \mathbf{-2\ V}$

f. $V_S = \mathbf{0\ V}$

Graphical Approach The resulting Shockley curve and the vertical line at $V_{GS} = -2\text{ V}$ are provided in Fig. It is certainly difficult to read beyond the second place without



Graphical solution for the network

$$V_{GS_Q} = -V_{GG} = \mathbf{-2\text{ V}}$$

b. $I_{D_Q} = \mathbf{5.6\text{ mA}}$

c. $V_{DS} = V_{DD} - I_D R_D = 16\text{ V} - (5.6\text{ mA})(2\text{ k}\Omega)$
$= 16\text{ V} - 11.2\text{ V} = \mathbf{4.8\text{ V}}$

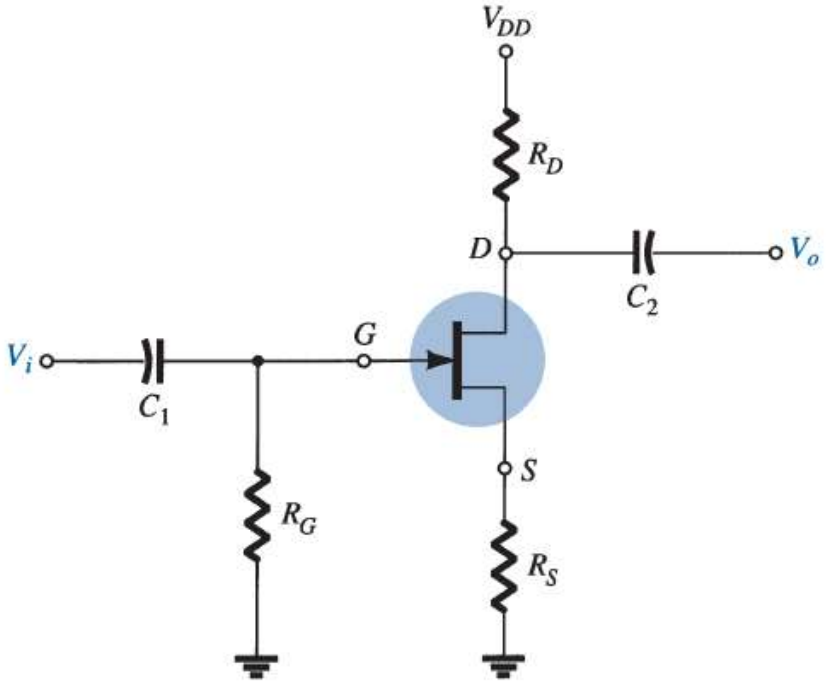
d. $V_D = V_{DS} = \mathbf{4.8\text{ V}}$

e. $V_G = V_{GS} = \mathbf{-2\text{ V}}$

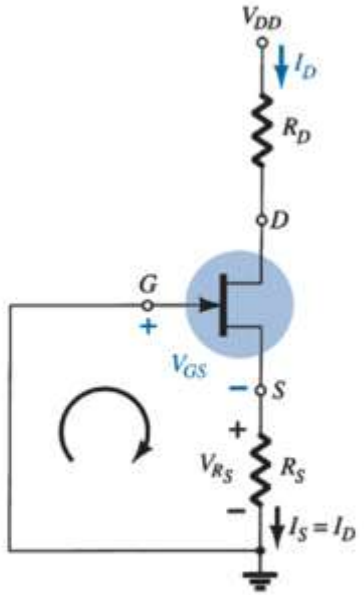
f. $V_S = \mathbf{0\text{ V}}$

Self-Bias Configuration:

The self-bias configuration eliminates the need for two dc supplies. The controlling gate-to-source voltage is now determined by the voltage across a resistor R_S introduced in the source leg of the configuration as shown in Fig.



JFET self-bias configuration.



DC analysis of the self-bias configuration.

For the dc analysis, the capacitors can again be replaced by “open circuits” and the resistor R_G replaced by a short-circuit equivalent since I_G = 0 A.

The current through R_S is the source current I_S, but $I_S = I_D$ and

$$V_{R_S} = I_D R_S$$

For the indicated closed loop of Fig. 9, we find that

$$-V_{GS} - V_{R_S} = 0$$

and

$$V_{GS} = -V_{R_S}$$

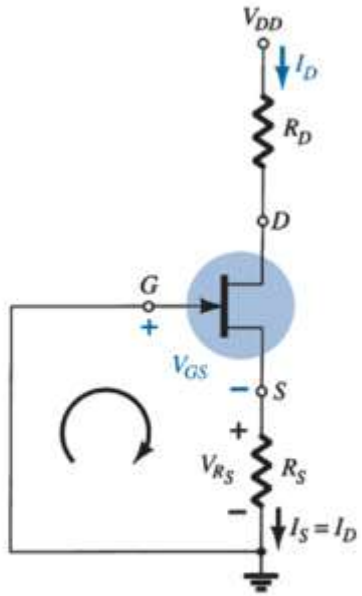
or

$$\boxed{V_{GS} = -I_D R_S}$$

Note in this case that *VGS* is a function of the output current *ID* and not fixed in magnitude as occurred for the fixed-bias configuration.

Drain Current (I_D) can be calculated from Shockley equation

using mathematical or a graphical Approach.



DC analysis of the self-bias configuration.

A mathematical solution could be obtained simply by substituting Eq. $V_{GS} = -I_D R_S$

in Shockley equation.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\left(1 - \frac{-I_D R_S}{V_P}\right)^2$$

or

$$I_D = I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$$

By performing the squaring process indicated and rearranging terms, we obtain an equation of the following form:

$$I_D^2 + K_1 I_D + K_2 = 0$$

The quadratic equation can then be solved for the appropriate solution for I_D.

The graphical approach:

- The graphical approach requires that we first establish the device transfer characteristics as shown in Fig.

$$V_{GS} = -I_D R_S$$

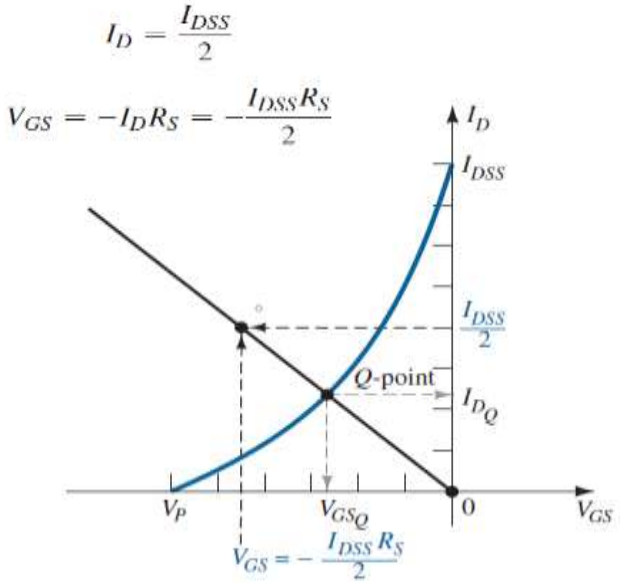


FIG.
Sketching the self-bias line.

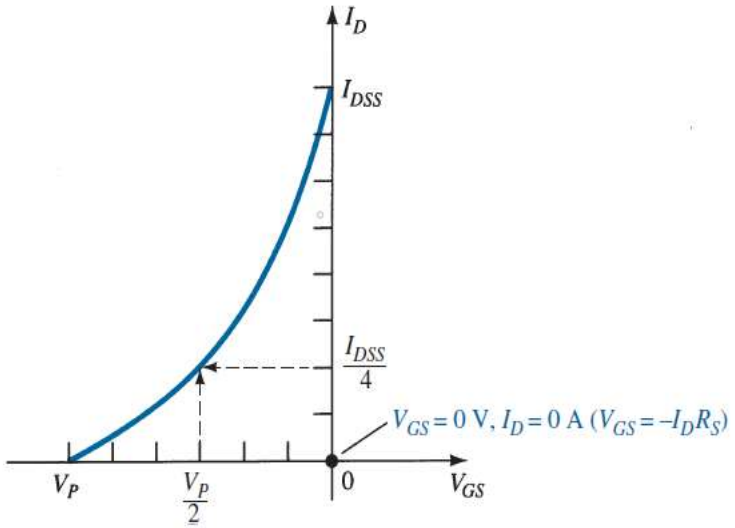


FIG.
Defining a point on the self-bias line.

The quiescent values of I_D and V_{GS} can then be determined and used to find the other quantities of interest.

The level of V_{DS} can be determined by applying Kirchhoff's voltage law to the output circuit, with the result that

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

and

$$V_{DS} = V_{DD} - V_{R_S} - V_{R_D} = V_{DD} - I_S R_S - I_D R_D$$

$$I_D = I_S$$

$$\boxed{V_{DS} = V_{DD} - I_D(R_S + R_D)}$$

$$\boxed{V_S = I_D R_S}$$

$$\boxed{V_G = 0\,\text{V}}$$

$$\boxed{V_D = V_{DS} + V_S = V_{DD} - V_{R_D}}$$

EXAMPLE 2 Determine the following for the network of Fig.

a. V_{GS_Q}.
b. I_{D_Q}.
c. V_{DS}.
d. V_S.
e. V_G.
f. V_D.

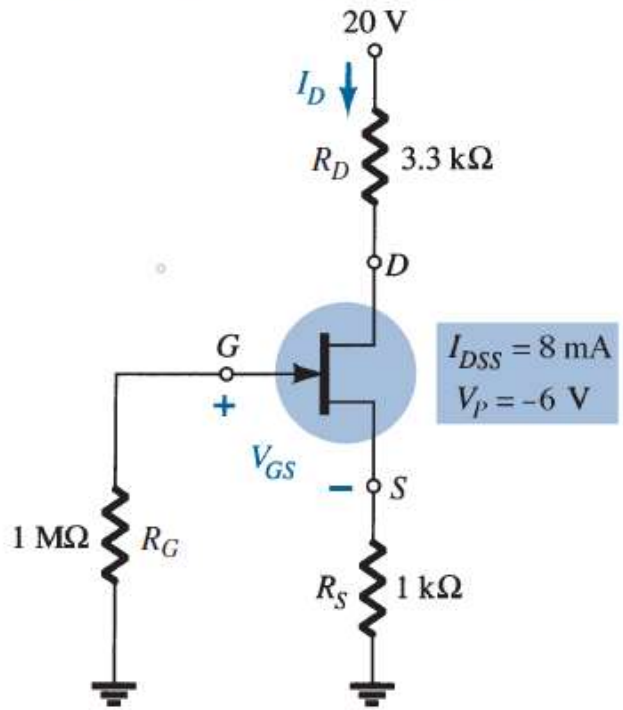


FIG.
Example 2.

Solution:

By using Graphical Method

a. The gate-to-source voltage is determined by

$$V_{GS} = -I_D R_S$$

Choosing $I_D = 4$ mA, we obtain

$$V_{GS} = -(4\text{ mA})(1\text{ k}\Omega) = -4\text{ V}$$

$$V_{GS_Q} = \mathbf{-2.6\text{ V}}$$

$$I_{D_Q} = \mathbf{2.6\text{ mA}}$$

If we happen to choose $I_D = 8$ mA, the resulting value of V_{GS} would be -8 V,

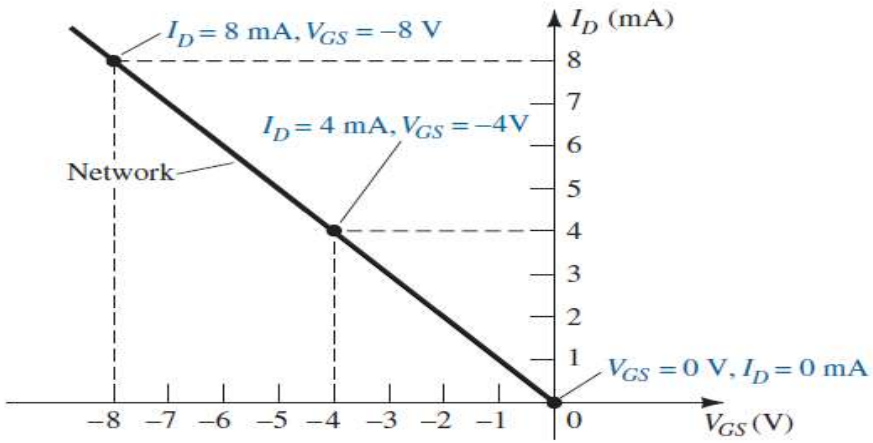


FIG.
Sketching the self-bias line for the network

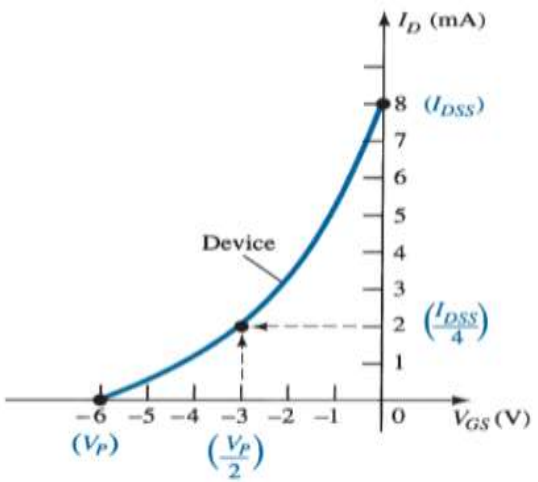


FIG.
Sketching the device characteristics for the JFET

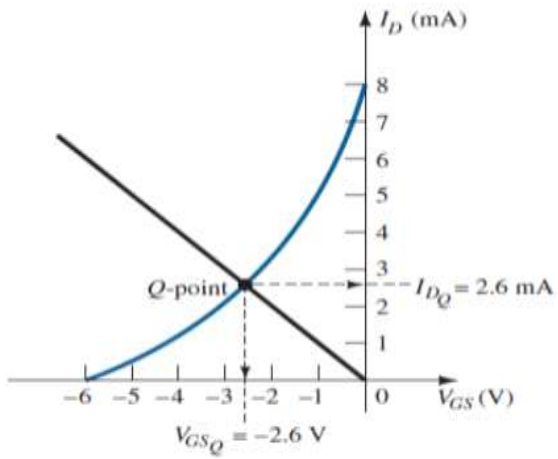


FIG.
Determining the Q-point for the network of

From the graphs $I_{D_Q} = \mathbf{2.6\ mA}$ $V_{GS_Q} = \mathbf{-2.6\ V}$

$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$
$$= 20\ \text{V} - (2.6\ \text{mA})(1\ \text{k}\Omega + 3.3\ \text{k}\Omega)$$
$$= 20\ \text{V} - 11.18\ \text{V}$$
$$= \mathbf{8.82\ V}$$

$$V_S = I_D R_S$$
$$= (2.6\ \text{mA})(1\ \text{k}\Omega)$$
$$= \mathbf{2.6\ V}$$
$$V_G = \mathbf{0\ V}$$
$$V_D = V_{DS} + V_S = 8.82\ \text{V} + 2.6\ \text{V} = \mathbf{11.42\ V}$$
$$V_D = V_{DD} - I_D R_D = 20\ \text{V} - (2.6\ \text{mA})(3.3\ \text{k}\Omega) = \mathbf{11.42\ V}$$

Voltage-Divider Biasing:

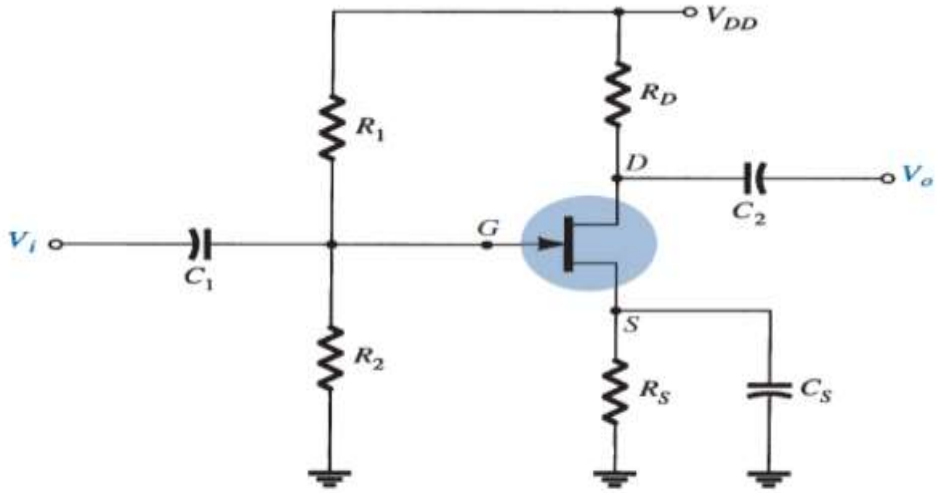


FIG.
Voltage-divider bias arrangement.

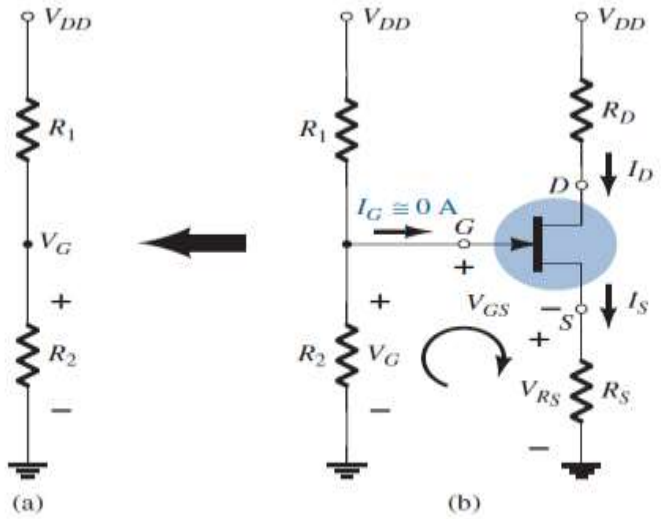


FIG.
Redrawn network for dc analysis.

The voltage V_G, equal to the voltage across R_2, can be found using the voltage-divider rule.

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Applying Kirchhoff's voltage law in the clockwise direction to the indicated loop

$$V_G - V_{GS} - V_{R_S} = 0$$

and

$$V_{GS} = V_G - V_{R_S}$$

Substituting $V_{R_S} = I_S R_S = I_D R_S$, we have

$$\boxed{V_{GS} = V_G - I_D R_S}$$

For one point I_D=0mA

$$V_{GS} = V_G - I_D R_S$$
$$= V_G - (0\text{ mA})R_S$$

$$\boxed{V_{GS} = V_G|_{I_D=0\text{ mA}}}$$

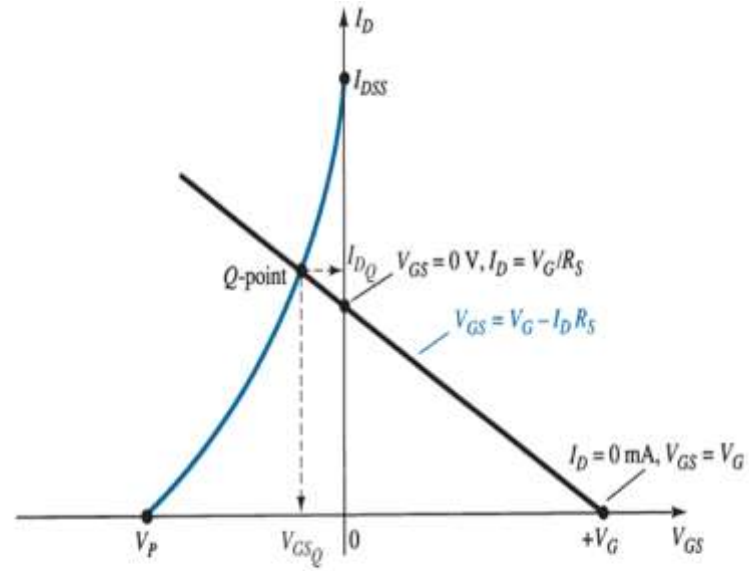


FIG.
Sketching the network equation for the voltage-divider configuration.

For the other point, let us now employ the fact that at any point on the vertical axis $V_{GS} = 0$ V and solve for the resulting value of I_D:

$$V_{GS} = V_G - I_D R_S$$
$$0\text{ V} = V_G - I_D R_S$$

and

$$\boxed{I_D = \frac{V_G}{R_S}\bigg|_{V_{GS}=0\text{ V}}}$$

Increasing values of R_S result in lower quiescent values of I_D and declining values of V_{GS}.

Once the quiescent values of I_{D_Q} and V_{GS_Q} are determined, the remaining network analysis can be performed in the usual manner. That is,

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

$$V_D = V_{DD} - I_D R_D$$

$$V_S = I_D R_S$$

$$I_{R_1} = I_{R_2} = \frac{V_{DD}}{R_1 + R_2}$$

Contents of the Class:

- FET small signal modelling
  - -Fixed bias
  - -Voltage divider bias

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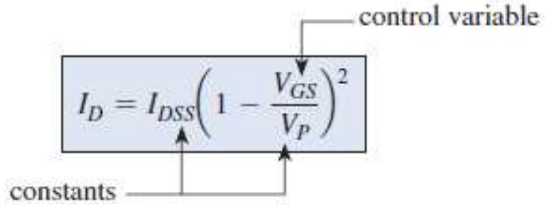
JFET small-signal Model:

- Field-effect transistor amplifiers provide an excellent voltage gain with the added feature of a high input impedance.
- The FET can be used as a linear amplifier or as a digital device in logic circuits.
- FET devices are also widely used in high-frequency applications and in buffering (interfacing) applications.
- Whereas the voltage gain of an FET amplifier is generally less than that obtained using a BJT amplifier, the FET amplifier provides a much higher input impedance than that of a BJT configuration.

JFET small-signal Model:

- The ac analysis of a JFET configuration requires that a small-signal ac model for the JFET be developed.
- ***The gate-to-source voltage controls the drain-to-source (channel) current of a JFET.***



Transcoductance(g_m)

- The *change* in drain current that will result from a *change* in gate-to-source voltage can be determined using the transconductance factor g_m in the following manner:

$$\Delta I_D = g_m \Delta V_{GS}$$

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

Mathematical definition of g_m

$$g_m = m = \frac{\Delta y}{\Delta x} = \frac{\Delta I_D}{\Delta V_{GS}}$$

If we therefore take the derivative of I_D with respect to V_{GS} (differential calculus) using Shockley's equation, we can derive an equation for g_m as follows:

$$g_m = \left.\frac{dI_D}{dV_{GS}}\right|_{Q\text{-pt.}} = \frac{d}{dV_{GS}}\left[I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2\right]$$

$$= I_{DSS}\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)$$

$$= 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\left[\frac{d}{dV_{GS}}(1) - \frac{1}{V_P}\frac{dV_{GS}}{dV_{GS}}\right] = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\left[0 - \frac{1}{V_P}\right]$$

and

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right]$$

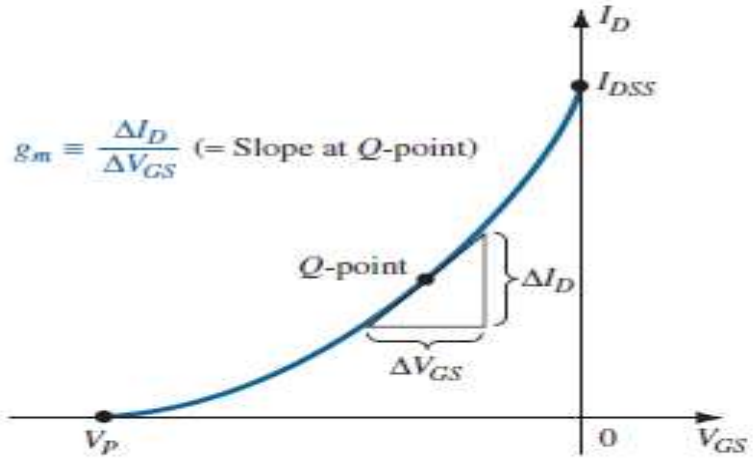


FIG.
Definition of g_m using transfer characteristic.

- Plugging in *VGS* = 0 V into the below Eq. results in the following equation for the maximum value of *gm* for a JFET in which *IDSS* and *VP* have been specified:

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right]$$

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{0}{V_P}\right]$$

$$g_{m0} = \frac{2I_{DSS}}{|V_P|}$$

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right]$$

Input impedance *Zi of JFET:*

The input impedance of all commercially available JFETs is sufficiently large. $Z_i\,(\text{JFET}) = \infty\,\Omega$

For a JFET a practical value of $10^9\ \Omega$ (1000 MΩ) is typical, whereas a value of $10^{12}\ \Omega$ to $10^{15}\ \Omega$ is typical for MOSFETs and MESFETs.

Output impedance *Zo Of JFET:*

$$Z_o\,(\text{JFET}) = r_d = \frac{1}{g_{os}} = \frac{1}{y_{os}}$$

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=\text{constant}}$$

The parameter y_{os} is a component of an *admittance equivalent circuit*, with the subscript *o* signifying an *o*utput network parameter and *s* the terminal (*s*ource) to which it is attached in the model.

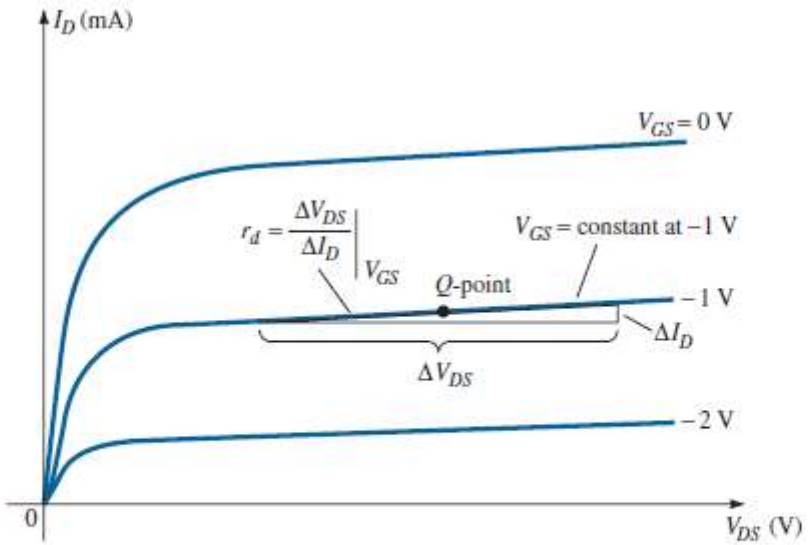


FIG.
Definition of r_d using JFET drain characteristics.

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}\Big|_{V_{GS}=\text{constant}}$$

The output impedance is defined on the characteristics of Fig. as the slope of the horizontal characteristic curve at the point of operation. The more horizontal the curve, the greater is the output impedance.

JFET AC Equivalent Circuit:

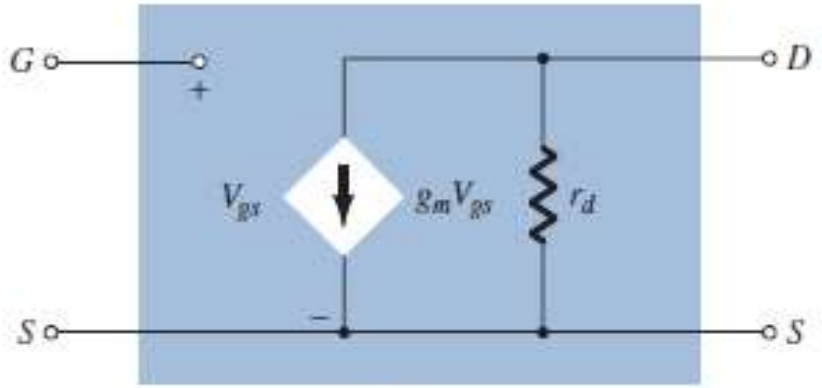


FIG.
JFET ac equivalent circuit.

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right]$$

$$Z_o\,(\text{JFET}) = r_d = \frac{1}{g_{os}} = \frac{1}{y_{os}}$$

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=\text{constant}}$$

The equivalent circuit is simply a current source whose magnitude is controlled by the signal V_{gs} and parameter g_m—clearly a voltage-controlled current source parallel with output impedance r_d.

AC analysis of JFET: 1)Fixed-Bias Configuration

The approach parallels the ac analysis of BJT amplifiers with a determination of the important parameters of Z_i, Z_o, and A_v for each configuration.

g_m and r_d are determined from the dc biasing arrangement

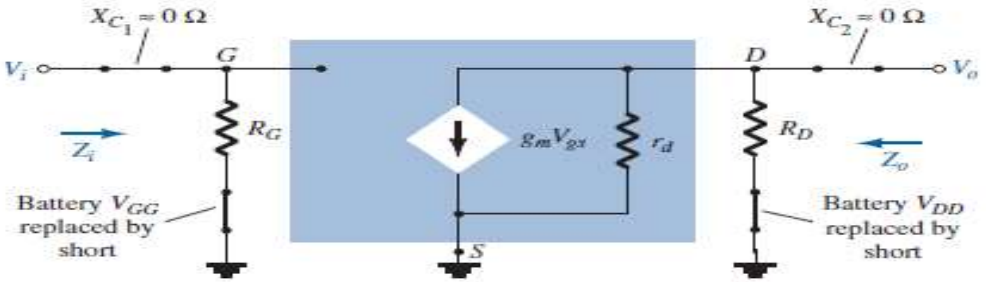


FIG.
Substituting the JFET ac equivalent circuit unit into the network

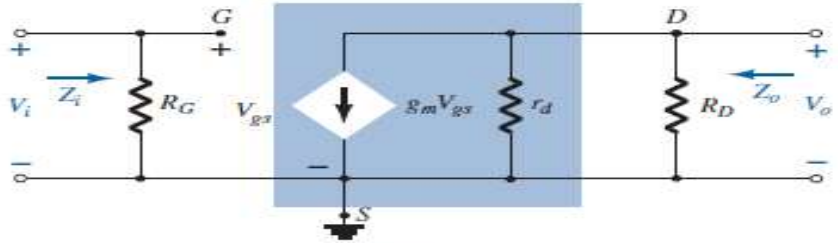


FIG.
Redrawn network

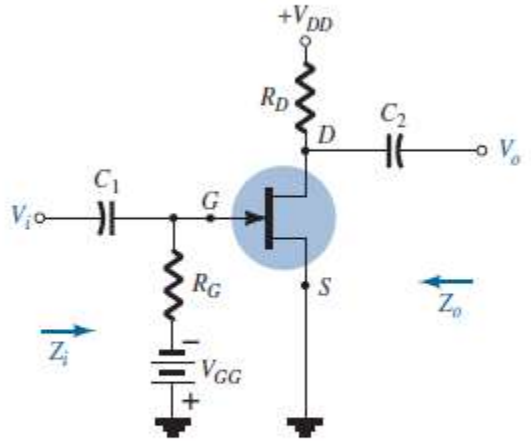
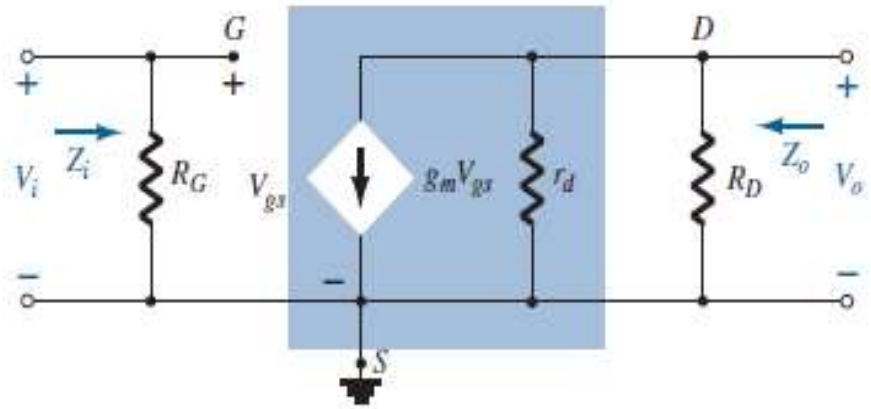


FIG.
JFET fixed-bias configuration.

Input impedance *Zi of JFET:*

$$Z_i = R_G$$

the infinite input impedance at the input terminals of the JFET.



Output impedance Zo *Of JFET:*

Z_o Setting $V_i = 0$ V as required by the definition of Z_o will establish V_{gs} as 0 V also. The result is $g_m V_{gs} = 0$ mA, and the current source can be replaced by an open-circuit equivalent . The output impedance is

$$Z_o = R_D \| r_d$$

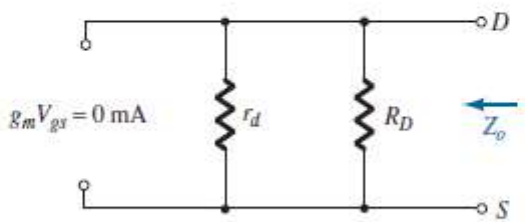


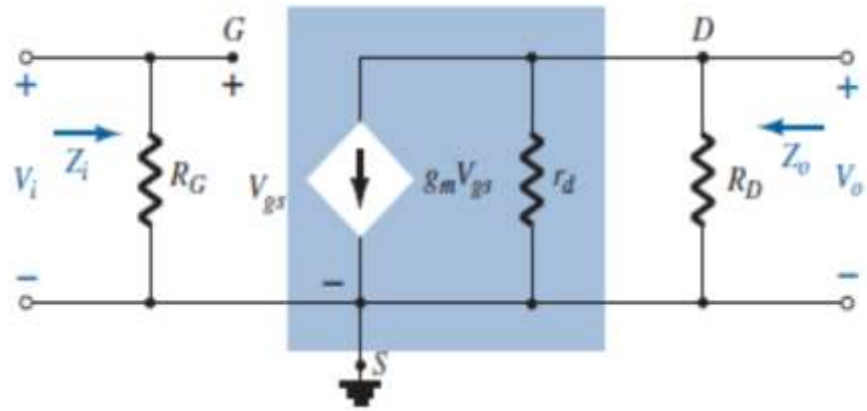
FIG. .
Determining Z_o

A_v Solving for V_o in Fig. we find

$$V_o = -g_m V_{gs}(r_d \| R_D)$$

but $$V_{gs} = V_i$$

and $$V_o = -g_m V_i(r_d \| R_D)$$



so that

$$A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)$$

If $r_d \geq 10R_D$,

$$A_v = \frac{V_o}{V_i} = -g_m R_D \qquad r_d \geq 10R_D$$

EXAMPLE The fixed-bias configuration of Example 1 had an operating point defined by $V_{GS_Q} = -2$ V and $I_{D_Q} = 5.625$ mA, with $I_{DSS} = 10$ mA and $V_P = -8$ V. The network is redrawn as Fig. with an applied signal V_i. The value of y_{os} is provided as 40 μS.

a. Determine g_m.
b. Find r_d.
c. Determine Z_i.
d. Calculate Z_o.
e. Determine the voltage gain A_v.
f. Determine A_v ignoring the effects of r_d.

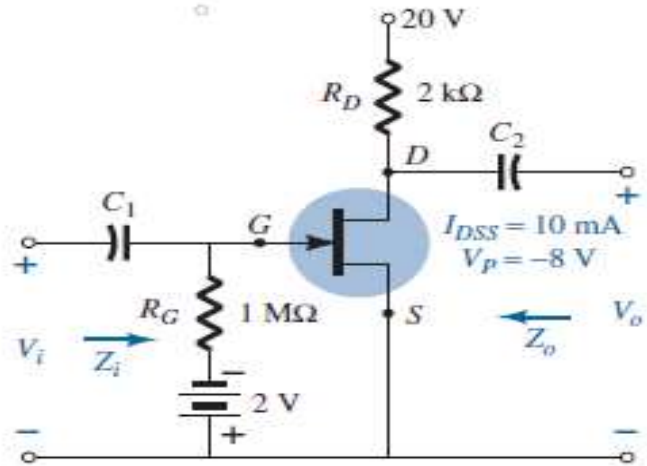


FIG.
JFET configuration for Example

Solution:

a. $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(10\text{ mA})}{8\text{ V}} = 2.5\text{ mS}$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 2.5\text{ mS}\left(1 - \frac{(-2\text{ V})}{(-8\text{ V})}\right) = \mathbf{1.88\text{ mS}}$$

b. $r_d = \dfrac{1}{y_{os}} = \dfrac{1}{40\ \mu\text{S}} = \mathbf{25\ k\Omega}$

c. $Z_i = R_G = \mathbf{1\ M\Omega}$

d. $Z_o = R_D \| r_d = 2\text{ k}\Omega \| 25\text{ k}\Omega = \mathbf{1.85\ k\Omega}$

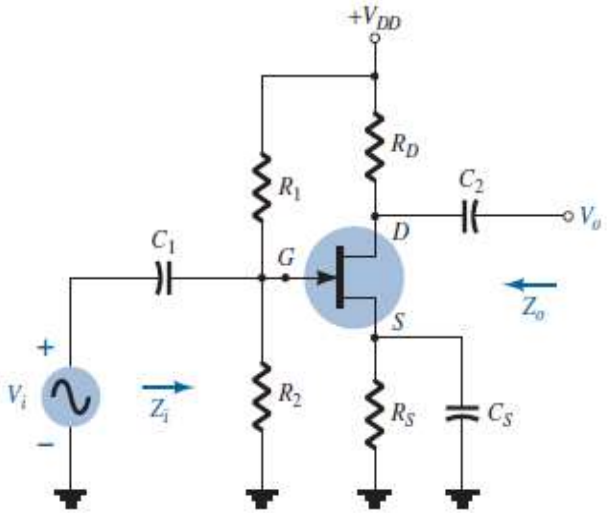
e. $A_v = -g_m(R_D \| r_d) = -(1.88\text{ mS})(1.85\text{ k}\Omega)$

$= \mathbf{-3.48}$

f. $A_v = -g_m R_D = -(1.88\text{ mS})(2\text{ k}\Omega) = \mathbf{-3.76}$

As demonstrated in part (f), a ratio of 25 kΩ:2 kΩ = 12.5:1 between r_d and R_D results in a difference of 8% in the solution.

Voltage Divider Bias:



JFET voltage-divider configuration.

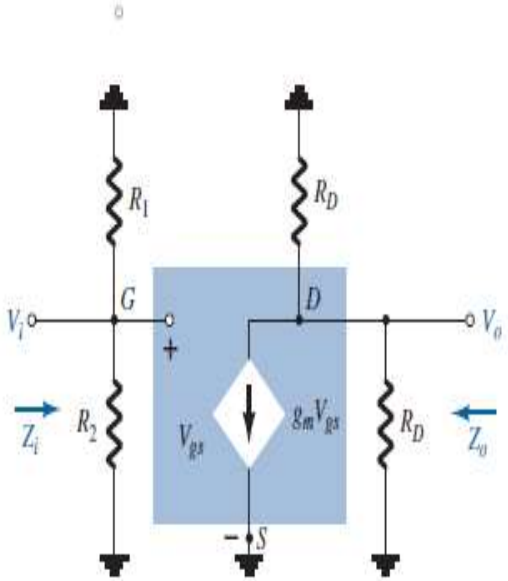


FIG.

Network of Fig. under ac conditions.

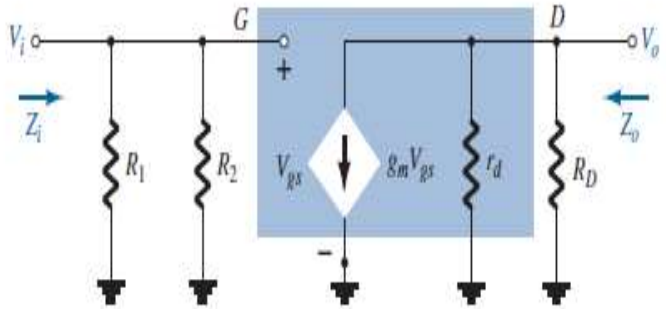


FIG.

Redrawn network

Z_i R_1 and R_2 are in parallel with the open-circuit equivalence of the JFET, resulting in

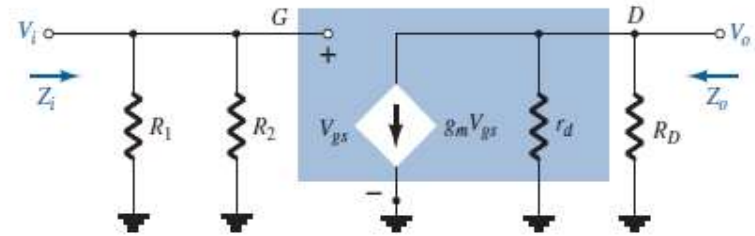
$$\boxed{Z_i = R_1 \| R_2}$$

Z_o Setting $V_i = 0$ V sets V_{gs} and $g_m V_{gs}$ to zero, and

$$\boxed{Z_o = r_d \| R_D}$$

For $r_d \geq 10R_D$,

$$\boxed{Z_o \cong R_D} \quad r_d \geq 10R_D$$



A_v

$$V_{gs} = V_i$$

and

$$V_o = -g_m V_{gs}(r_d \| R_D)$$

so that

$$A_v = \frac{V_o}{V_i} = \frac{-g_m V_{gs}(r_d \| R_D)}{V_{gs}}$$

and

$$\boxed{A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)}$$

If $r_d \geq 10R_D$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong -g_m R_D} \quad r_d \geq 10R_D$$

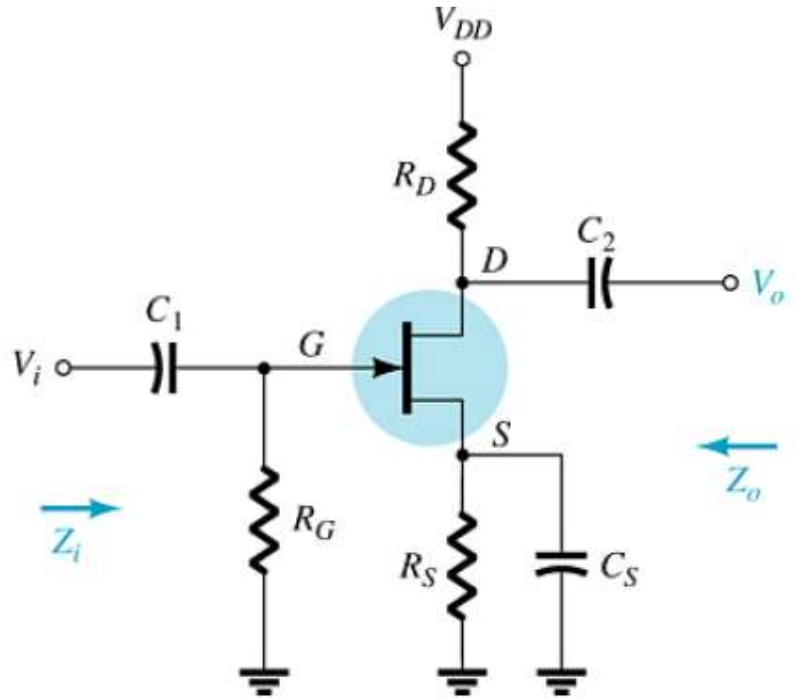
Contents of the class:

- Common-Source (CS) Self-Bias Circuit
- Effect of R_L and R_{sig} in JFET amplifiers
- Cascade Configuration of JFET Amplifier
- Frequency response of an amplifier-Bode plot
- RC-Coupled amplifier and its low frequency response.

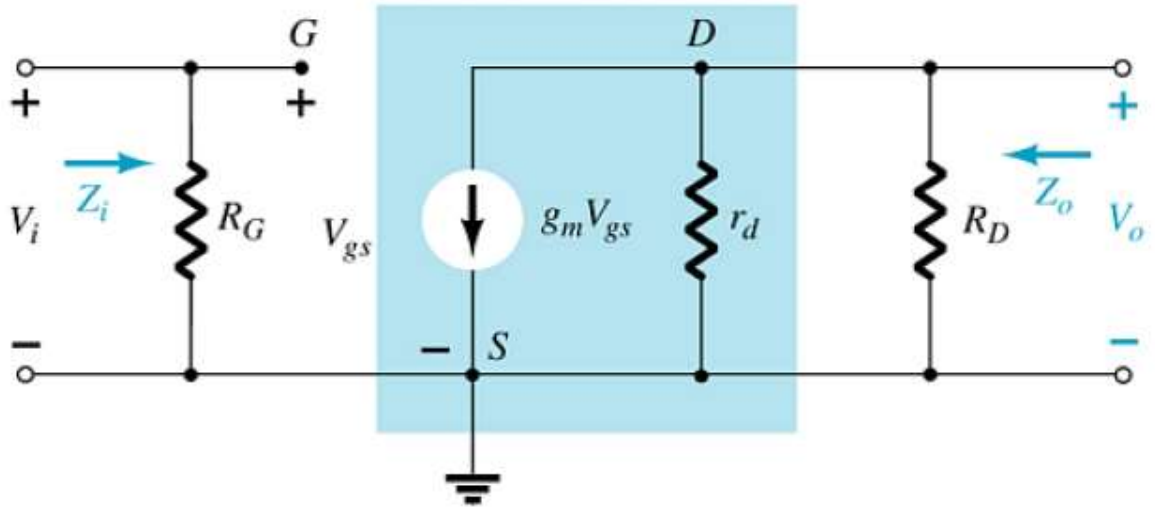
Reference:Electronics devices and circuit Theory by R L Boylestad

Common-Source (CS) Self-Bias Circuit - Bypassed R_S

- This is a common-source amplifier configuration, so the input is on the gate and the output is on the drain.
- There is a 180° phase shift between input and output.



Bypassed R_S



Common-Source (CS) Self-Bias Circuit - Bypassed R_S

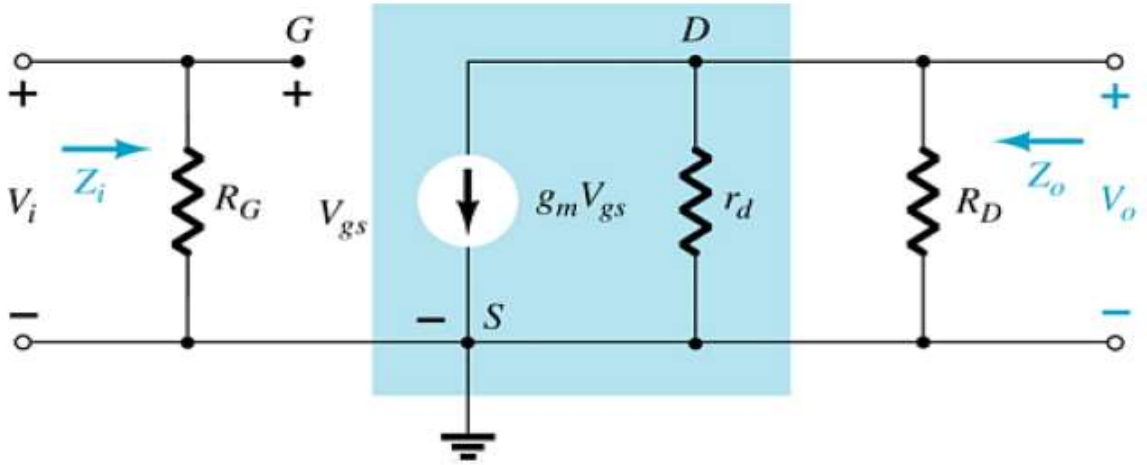
Input impedance:

$$Z_i = R_G$$

Output impedance:

$$Z_o = r_d \parallel R_D$$

$$Z_o \cong R_D \Big|_{r_d \geq 10R_D}$$



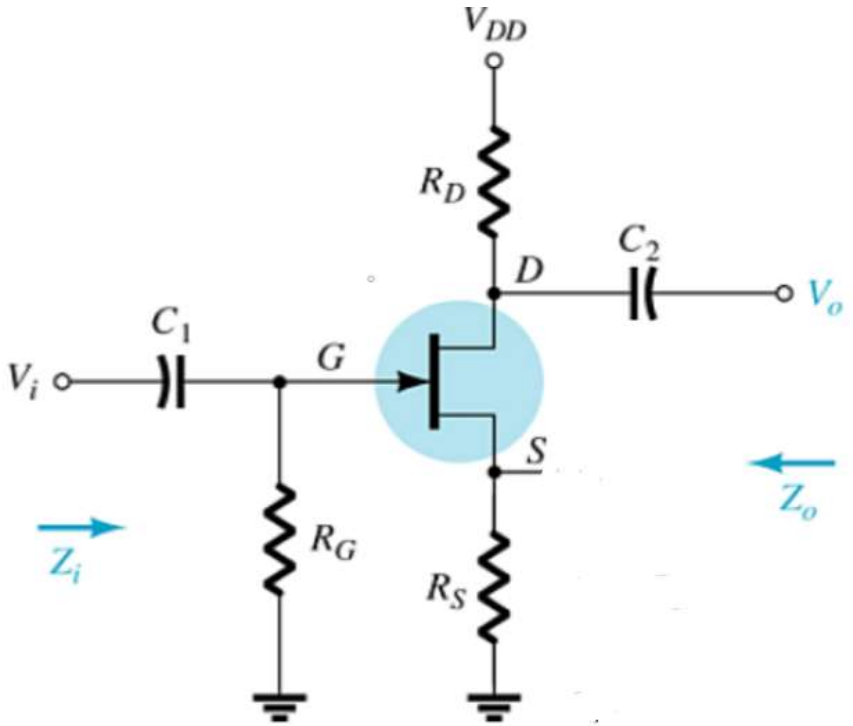
Voltage gain:

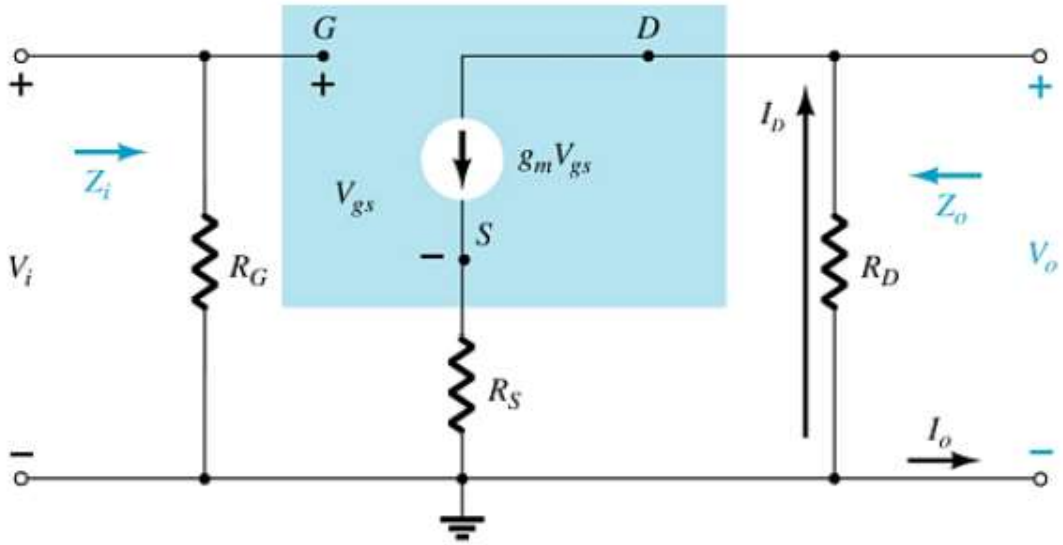
$$A_v = -g_m (r_d \parallel R_D)$$

$$A_v = -g_m R_D \Big|_{r_d \geq 10R_D}$$

Common-Source (CS) Self-Bias Circuit - Unbypassed R_S

Removing C_S affects the gain of the circuit.





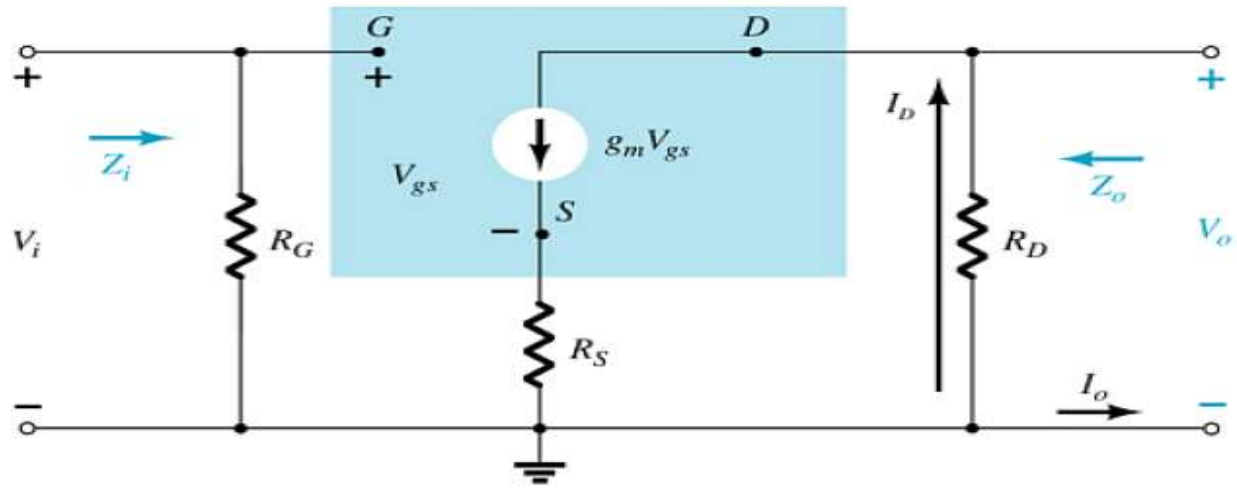
Common-Source (CS) Self-Bias Circuit - Unbypassed R_S

Input impedance:

$$Z_i = R_G$$

Output impedance:

$$Z_o \cong R_D \Big|_{r_d \geq 10R_D}$$



Voltage gain:

$$A_v = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}}$$

$$A_v = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S}\Bigg|_{r_d \geq 10(R_D + R_S)}$$

Effect of R_L and R_{sig} in JFET amplifiers:

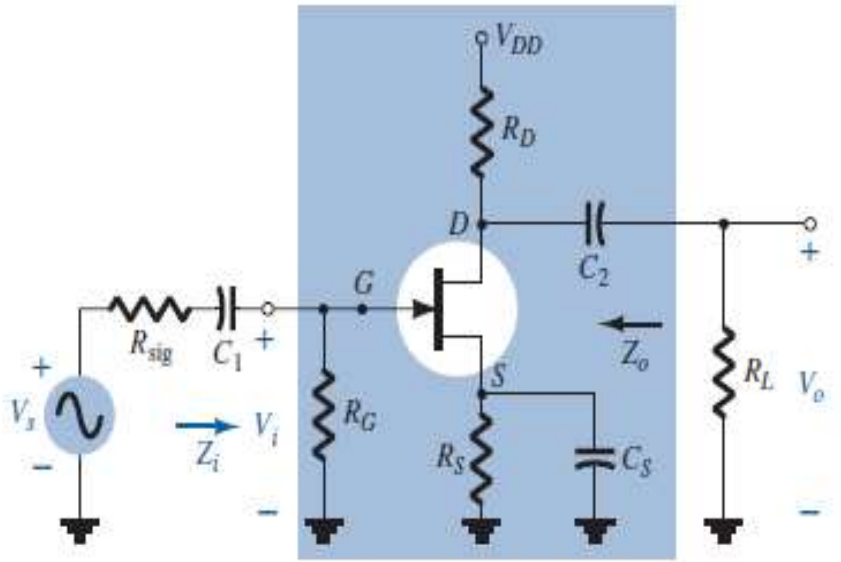
$$A_{v_L} = \frac{R_L}{R_L + R_o} A_{v_{NL}}$$

$$A_i = -A_{v_L} \frac{Z_i}{R_L}$$

$$A_{v_s} = \frac{V_o}{V_s} = \frac{V_i}{V_s} \cdot \frac{V_o}{V_i} = \left(\frac{R_i}{R_i + R_{sig}}\right)\left(\frac{R_L}{R_L + R_o}\right) A_{v_{NL}}$$

The greatest gain of an amplifier is the no-load gain.
The loaded gain is always less than the no-load gain.
A source impedance will always reduce the overall gain below the no-load or loaded level.

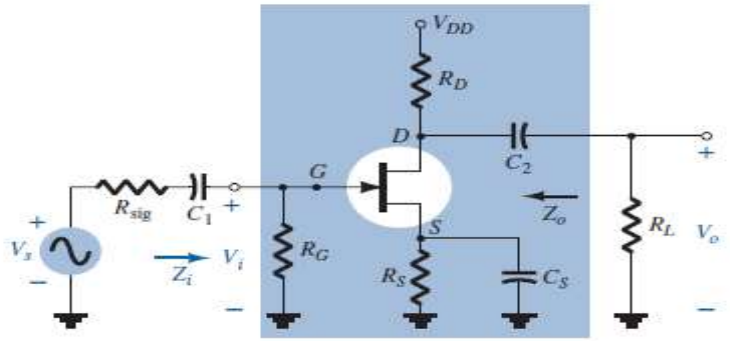
$$A_{v_{NL}} > A_{v_L} > A_{v_S}$$



JFET amplifier with R_{sig} and R_L.

The load resistance appears in parallel with the drain resistance and the source resistance R_{sig} appears in series with the gate resistance R. For the overall voltage gain the result is a modified form of

$$A_{v_L} = \frac{V_o}{V_i} = -g_m(r_d \| R_D \| R_L)$$



JFET amplifier with R_{sig} and R_L.

The output impedance is the same as obtained for the unloaded situation without a source resistance:

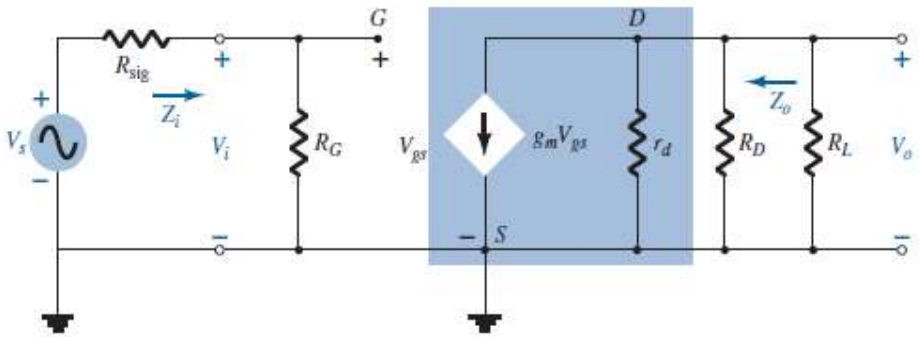
$$Z_o = r_d \| R_D$$

The input impedance remains as

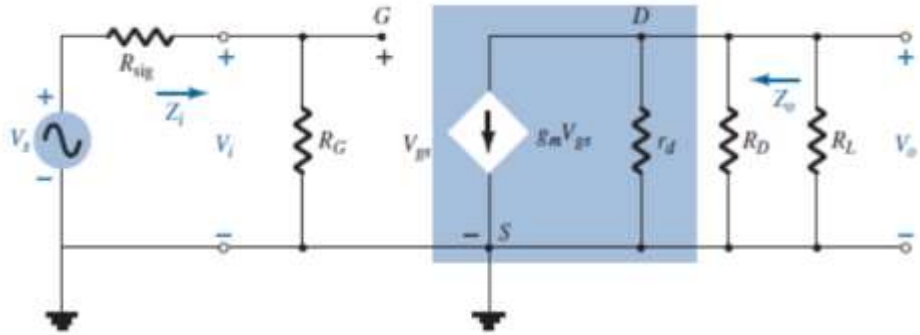
$$Z_i = R_G$$

For the overall gain A_{v_S},

$$V_i = \frac{R_G V_S}{R_G + R_{sig}}$$



the ac equivalent circuit for the JFET.



and

$$A_{v_S} = \frac{V_o}{V_s} = \frac{V_i}{V_s}\cdot\frac{V_o}{V_i} = \left[\frac{R_G}{R_G + R_{\text{sig}}}\right][-g_m(r_d \| R_D \| R_L)]$$

which for most applications where $R_G \gg R_{\text{sig}}$ and $R_D \| R_L \ll r_d$ results in

$$A_{v_S} \cong -g_m(R_D \| R_L)$$

If we now turn to the two-port approach for the same network, the equation for the overall gain becomes

$$A_{v_L} = \frac{R_L}{R_L + R_o}A_{v_{\text{NL}}} = \frac{R_L}{R_L + R_o}[-g_m(r_d \| R_D)]$$

but

$$R_o = R_D \| r_d,$$

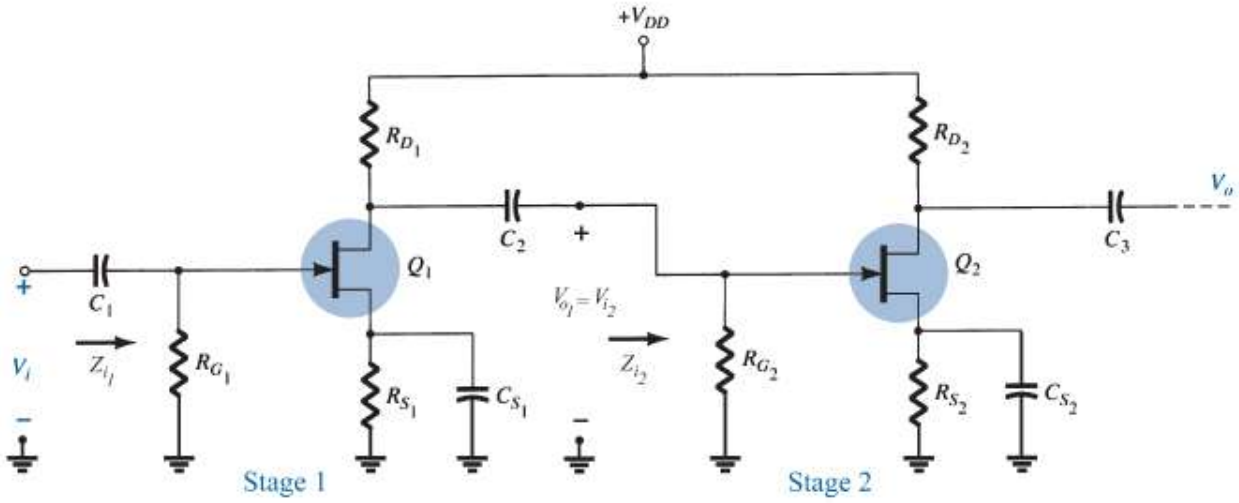
so that

$$A_{v_L} = \frac{R_L}{R_L + R_D \| r_d}[-g_m(r_d \| R_D] = -g_m\frac{(r_d \| R_D)(R_L)}{(r_d + R_D) + R_L}$$

and

$$A_{v_L} = -g_m(r_d \| R_D \| R_L)$$

Cascade Configuration of JFET Amplifier:



Cascaded FET amplifier.

The output of one stage appears as the input for the following stage. The input impedance for the second stage is the load impedance for the first stage.

The total gain is the product of the gain of each stage including the loading effects of the following stage.

$$A_v = A_{v_1}A_{v_2} = (-g_{m_1}R_{D_1})(-g_{m_2}R_{D_2}) = g_{m_1}g_{m_2}R_{D_1}R_{D_2}$$

Frequency response of an BJT amplifier :

The **frequency response** of an amplifier refers to the frequency range in which the amplifier will operate with negligible effects from capacitors and device internal capacitance. This range of frequencies can be called the **mid-range**.

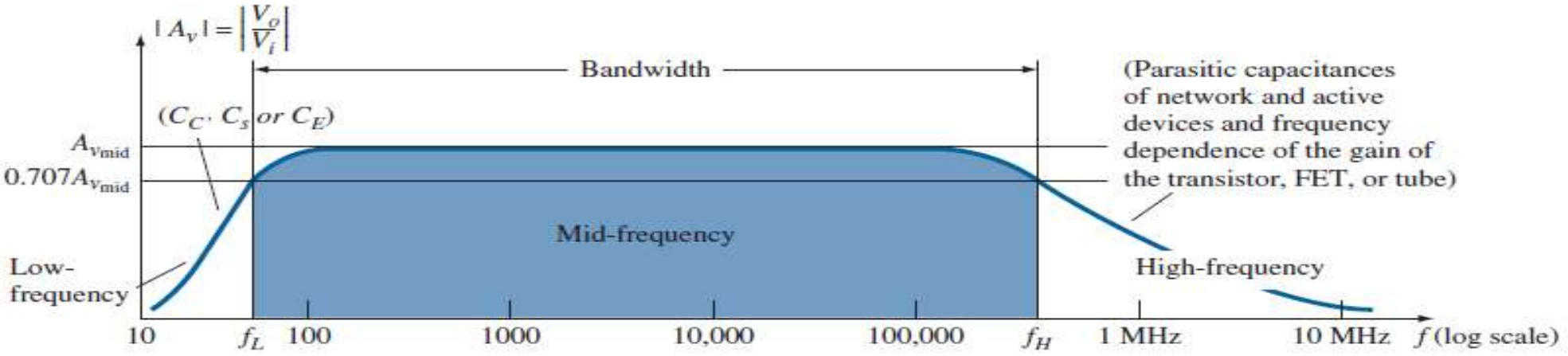
At frequencies above and below the midrange, capacitance and any inductance will affect the gain of the amplifier.

•At low frequencies the coupling and bypass capacitors lower the gain.

•At high frequencies stray capacitances associated with the active device lower the gain.

•Also, cascading amplifiers limits the gain at high and low frequencies.

Frequency response:



Gain versus frequency: RC-coupled amplifiers

A Bode plot indicates the frequency response of an amplifier.
The horizontal scale indicates the frequency (in Hz) and the vertical scale indicates the gain (in dB).

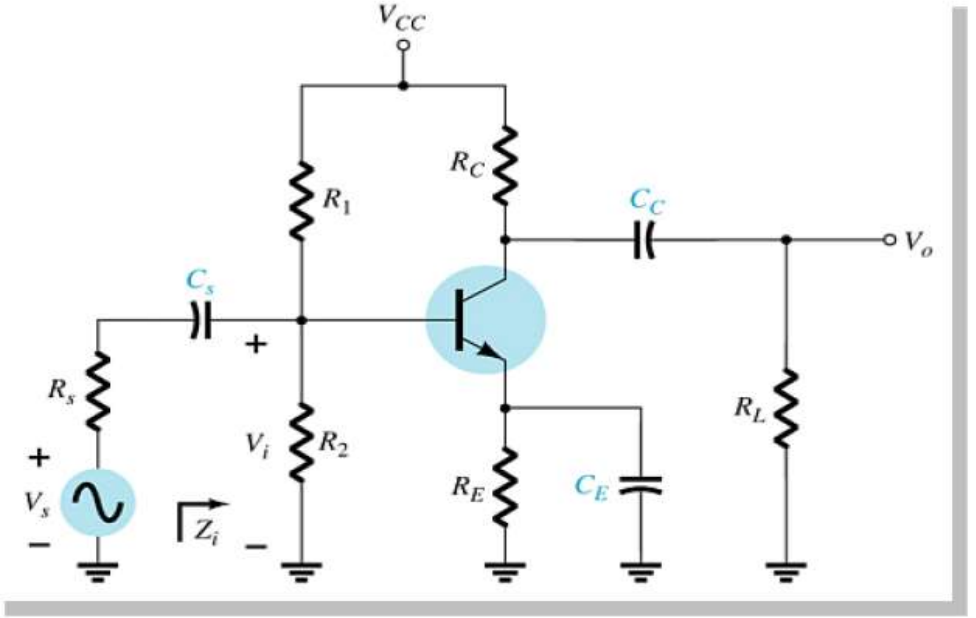
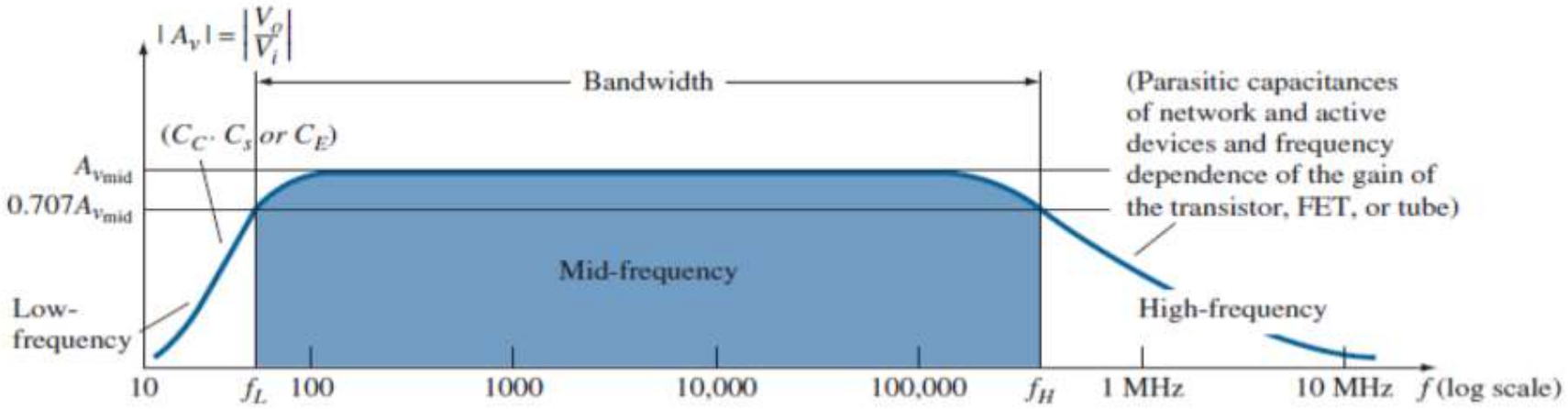


Fig: Common emitter Single stage RC-Coupled Amplifier

- **Frequencies: The mid-range frequency range of an amplifier is called the bandwidth of the amplifier.**

$$\text{bandwidth (BW)} = f_H - f_L$$

- **The bandwidth is defined by the lower and upper cutoff frequencies.**
- **Cutoff–any frequency at which the gain has dropped by 3 dB.**



BJT Amplifier Low-Frequency Response:

At low frequencies, coupling capacitor (C_S, C_C) and bypass capacitor (C_E) reactances affect the circuit impedances.

Coupling Capacitor (C_S)

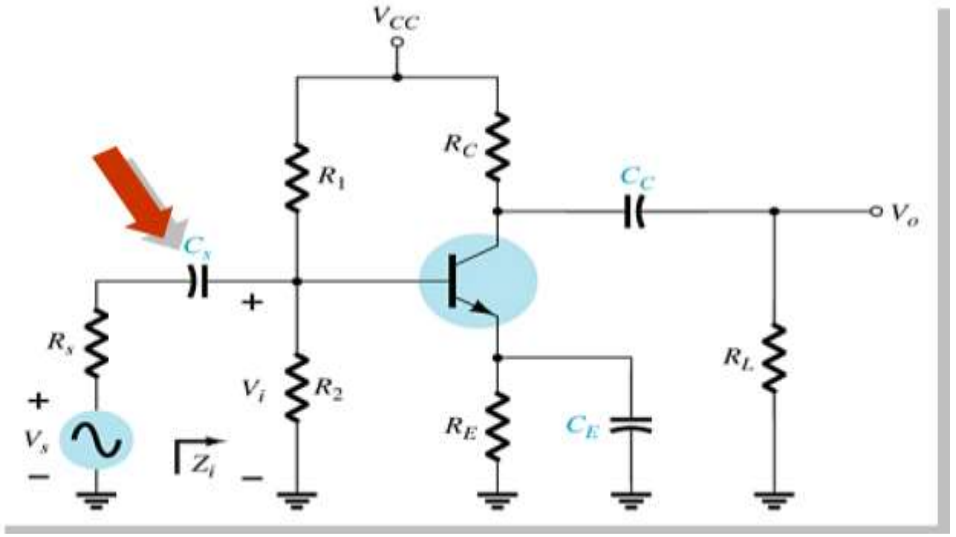
The cutoff frequency due to C_S can be calculated by

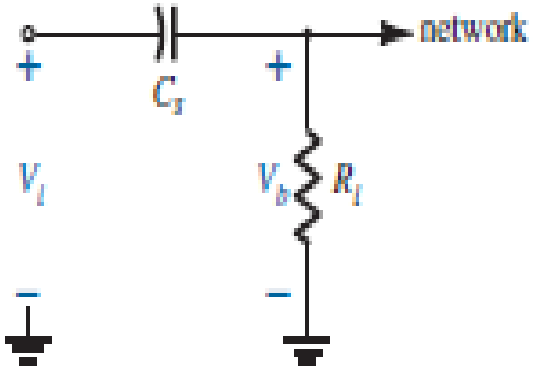
$$f_L = \frac{1}{2\pi RC}$$

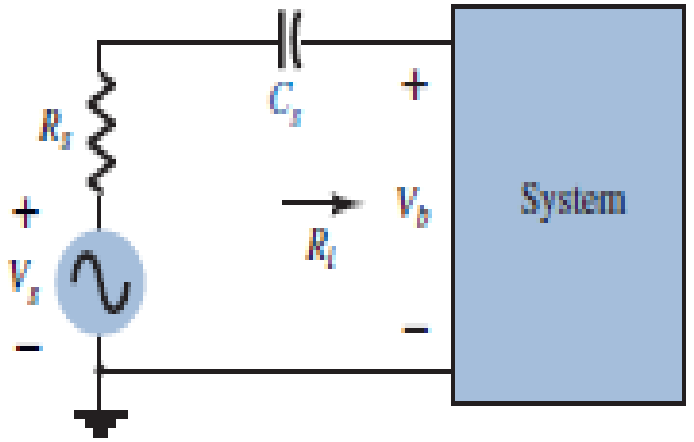
$$f_{Ls} = \frac{1}{2\pi(R_s + R_i)C_s}$$

where

$$R_i = R_1 \,||\, R_2 \,||\, \beta r_e$$







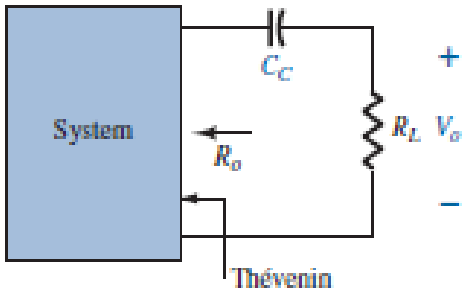
Coupling Capacitor (C_C) :

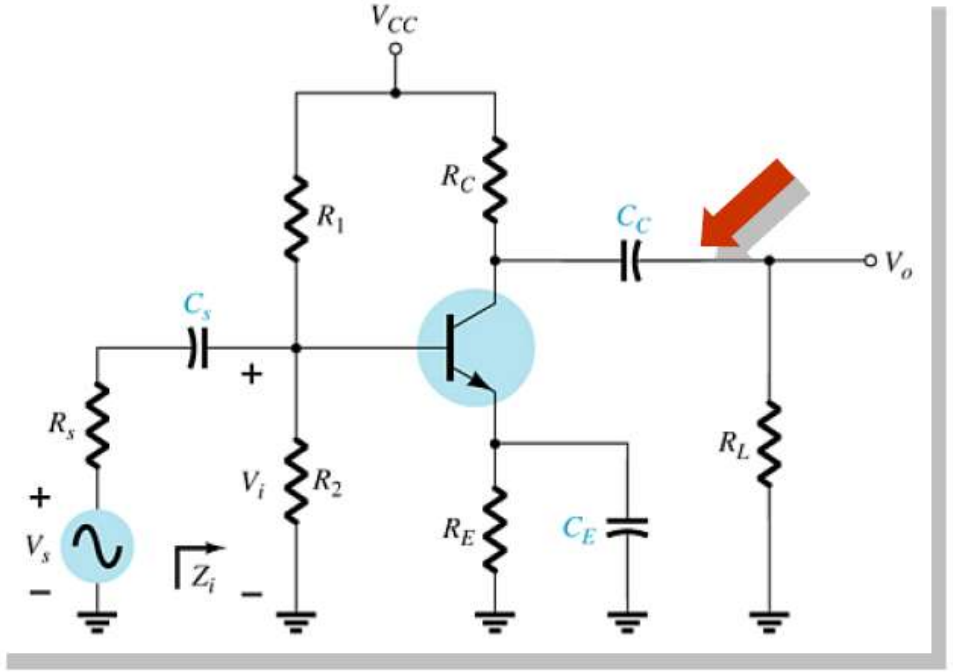
The cutoff frequency due to C_C can be calculated with

$$f_{LC} = \frac{1}{2\pi(R_o + R_L)C_c}$$

where

$$R_o = R_C \,||\, r_o$$





$$f_L = \frac{1}{2\pi RC}$$

Bypass Capacitor (C_E):

The cutoff frequency due to C_E can be calculated with

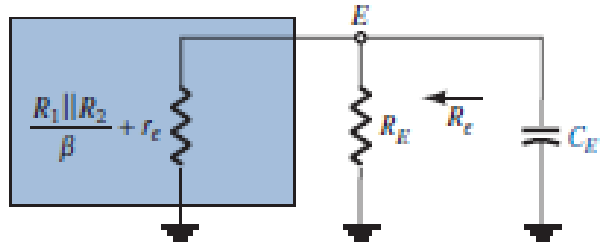
$$f_{LE} = \frac{1}{2\pi R_e C_E}$$

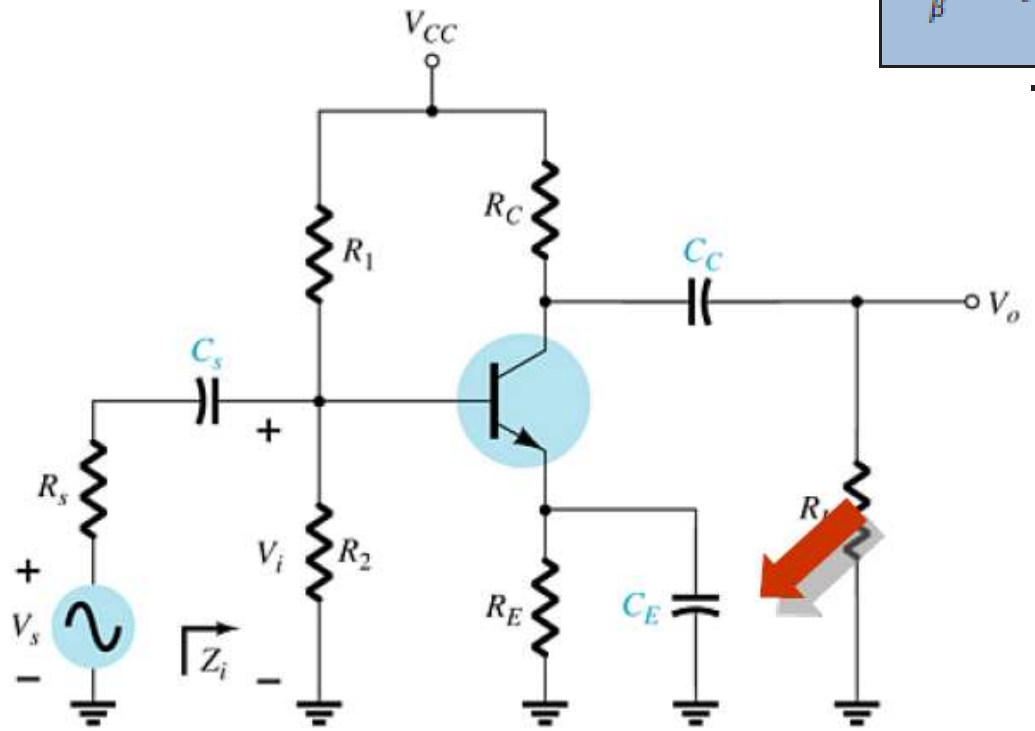
where

$$R_e = R_E \,||\, \left(\frac{R'_s}{\beta} + r_e\right)$$

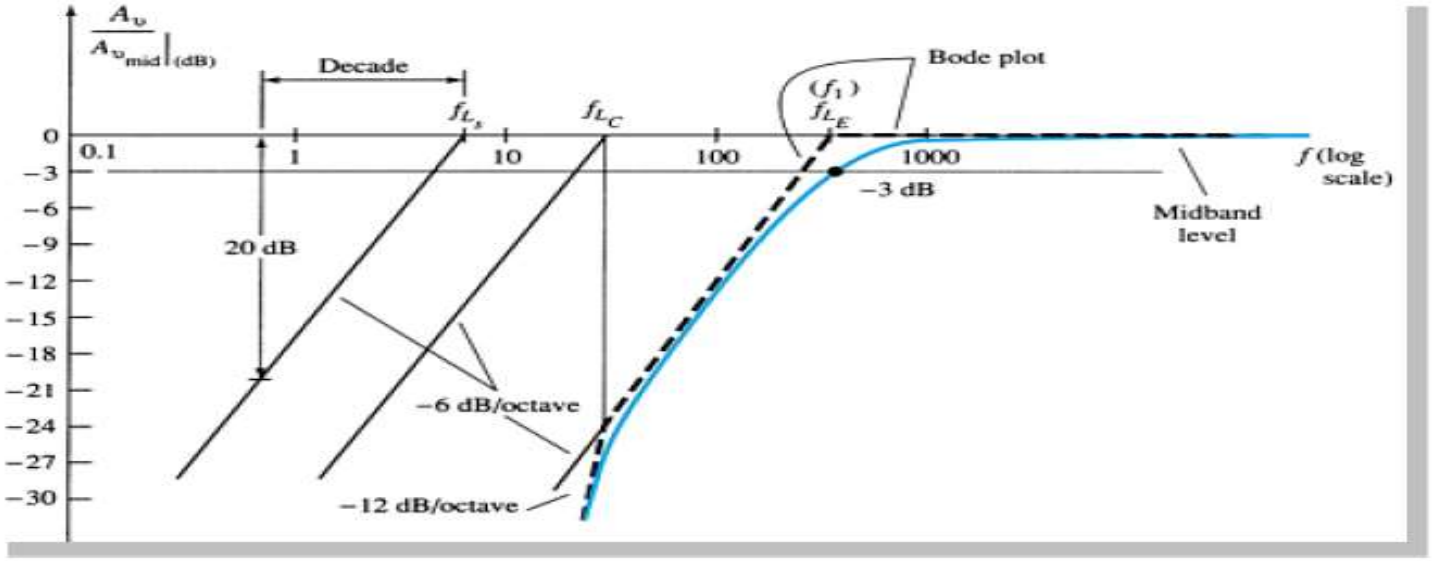
and

$$R'_s = R_s \,||\, R_1 \,||\, R_2$$





BJT Amplifier Low-Frequency Response:



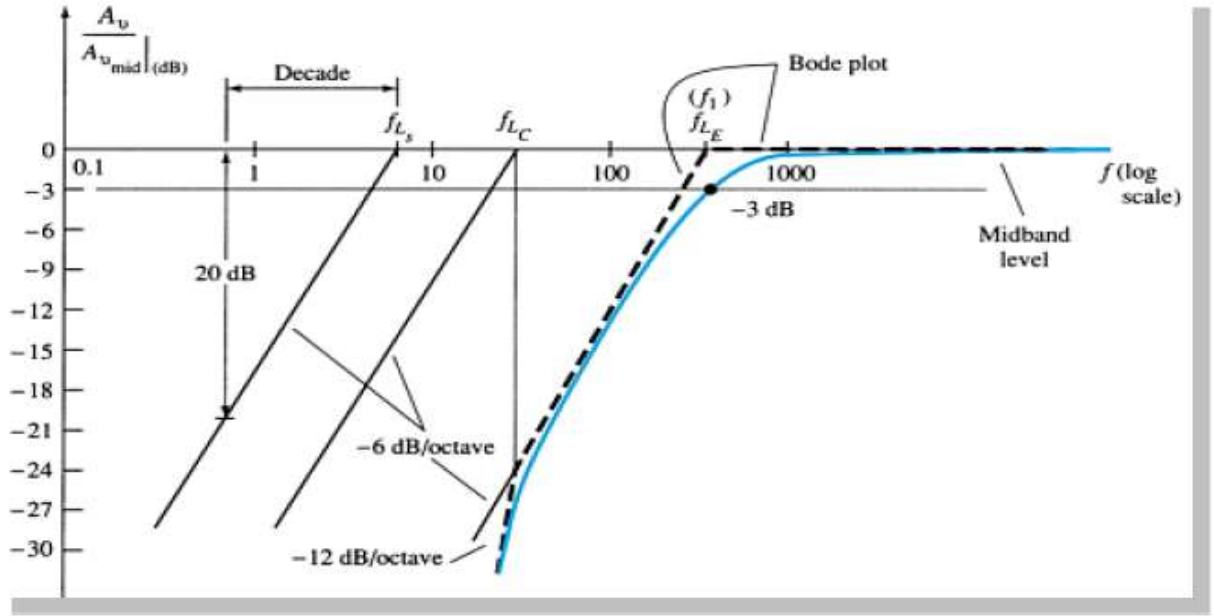
The <u>Bode plot</u> indicates that each capacitor may have a different cutoff frequency.
It is the device that has the *highest* lower cutoff frequency (f_L) that dominates the overall frequency response of the amplifier.

Roll-Off of Gain in the Bode Plot

The Bode plot not only indicates the cutoff frequencies of the various capacitors it also indicates the amount of attenuation (loss in gain) at these frequencies.

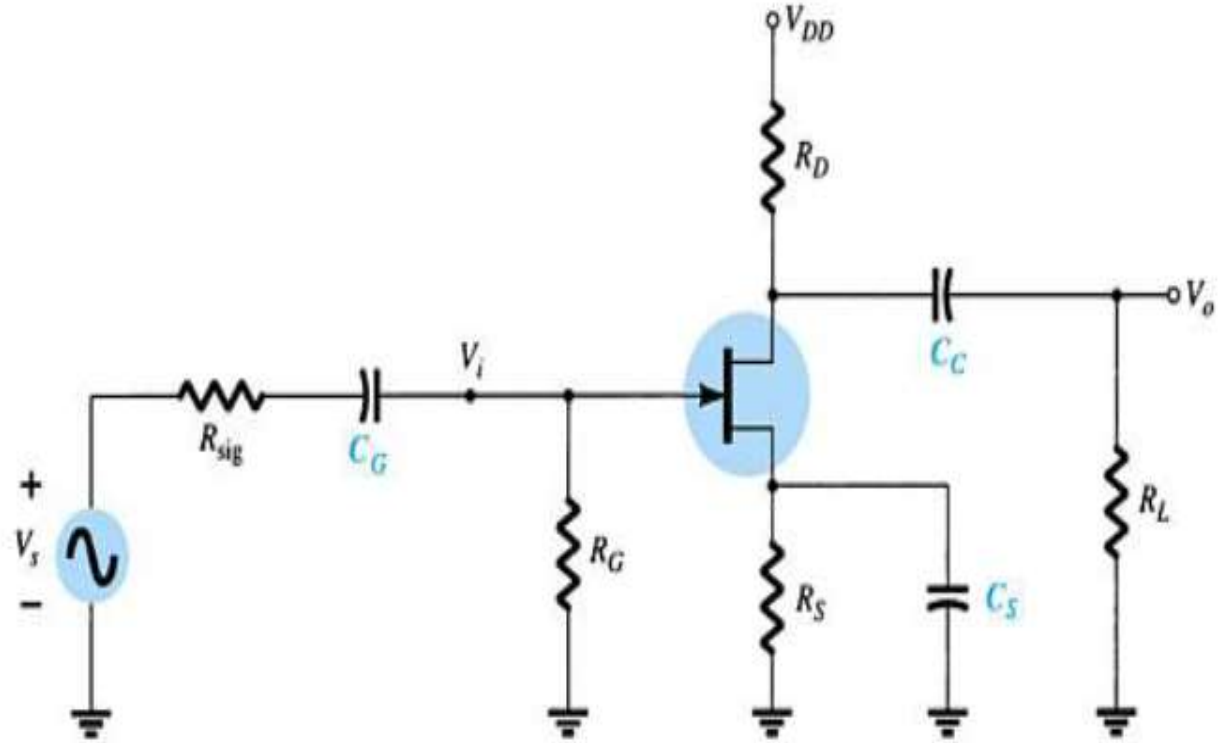
The amount of attenuation is sometimes referred to as roll-off.

The roll-off is described as dB loss-per-octave or dB loss-per-decade.



FET Amplifier Low-Frequency Response

At low frequencies, coupling capacitor (C_G, C_C) and bypass capacitor (C_S) reactances affect the circuit impedances.



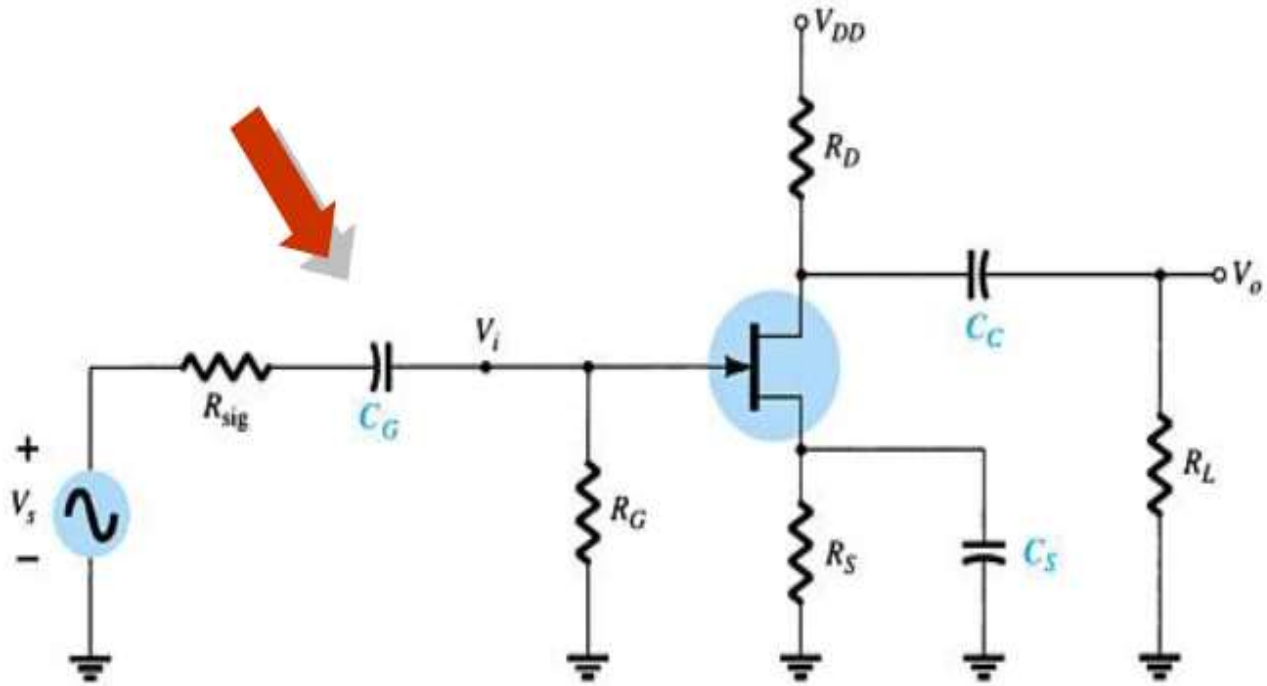
Coupling Capacitor (C_G)

The cutoff frequency due to C_G can be calculated with

$$f_{LC} = \frac{1}{2\pi(R_{sig} + R_i)C_G}$$

where

$$R_i = R_G$$



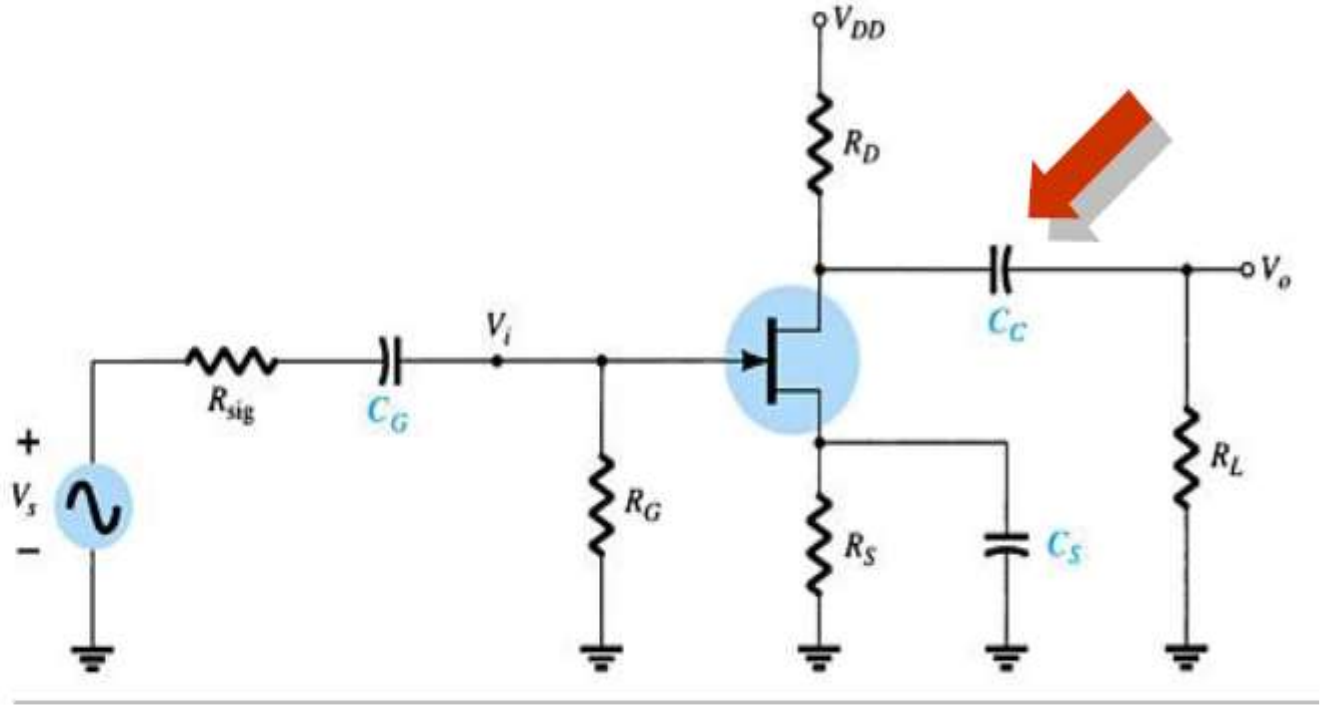
Coupling Capacitor (C_C)

The cutoff frequency due to C_C can be calculated with

$$f_{LC} = \frac{1}{2\pi(R_o+R_L)C_C}$$

where

$$R_o = R_D \,||\, r_d$$



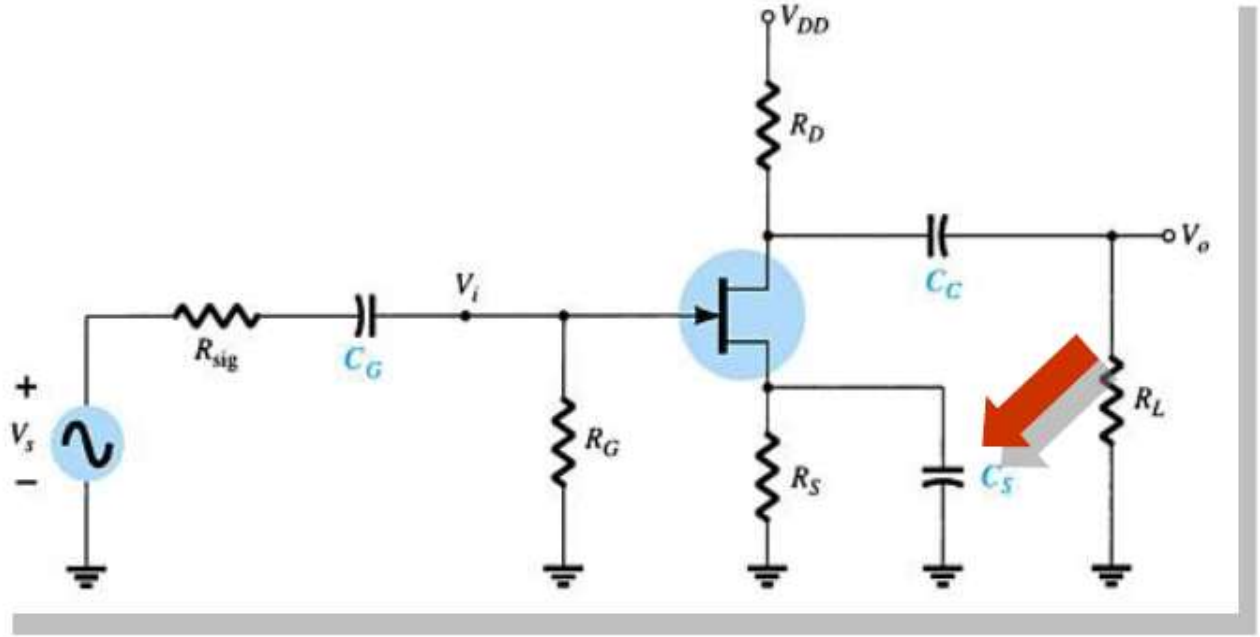
Bypass Capacitor (C_S)

The cutoff frequency due to C_S can be calculated with

$$f_{LS} = \frac{1}{2\pi R_{eq} C_S}$$

where

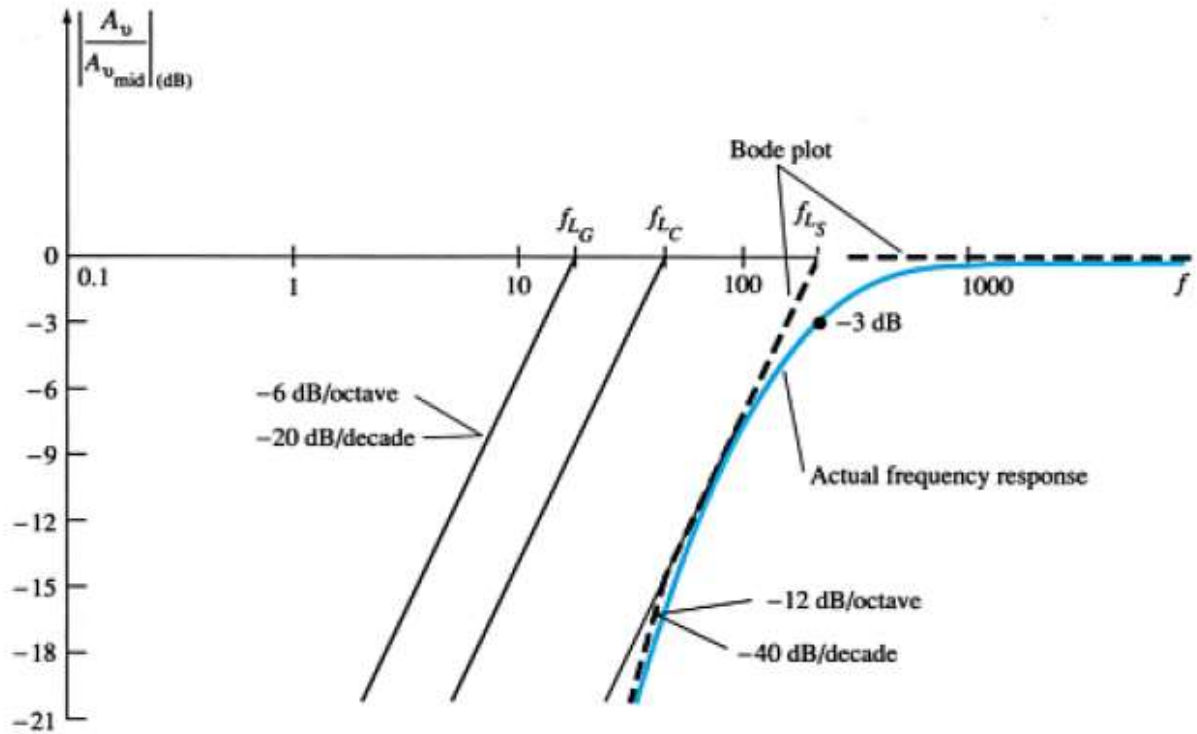
$$R_{eq} = R_S \,||\, \frac{1}{g_m}\Big|_{r_d \cong \infty\Omega}$$



FET Amplifier Low-Frequency Response

The Bode plot indicates that each capacitor may have a different cutoff frequency.

The capacitor that has the *highest* lower cutoff frequency (f_L) is closest to the actual cutoff frequency of the amplifier.



Thank you.

Contents of the Class:

- BJT Amplifier High-Frequency Response
- FET Amplifier High-Frequency Response
- Classification of amplifier,
- Feedback concept
- Negative feedback

- Referred Book:- R L Boylestad

Frequency response of an Amplifier

Frequencies: The mid-range frequency range of an amplifier is called the bandwidth of the amplifier.

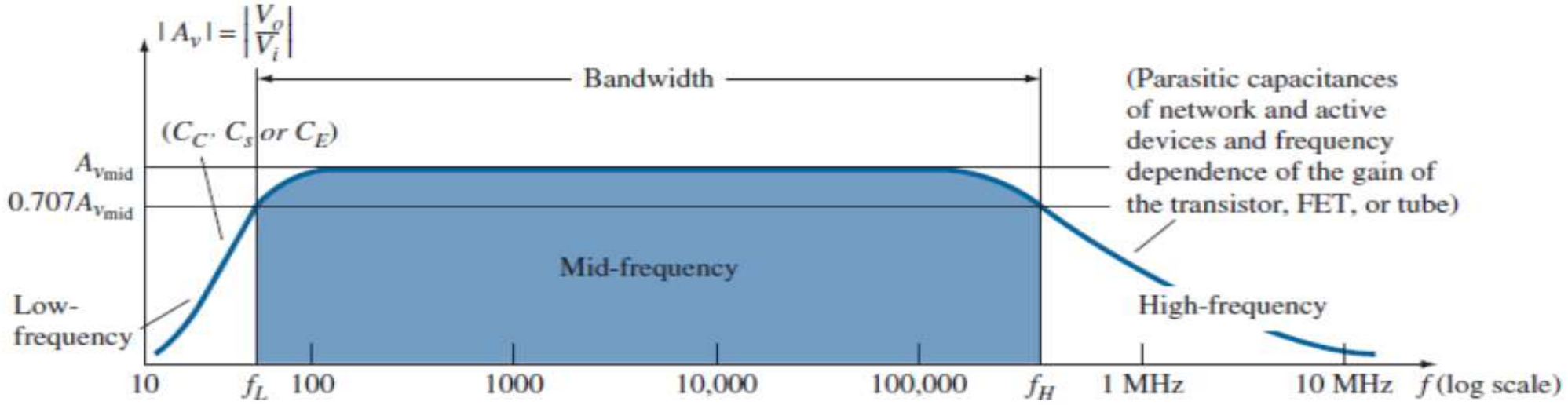
$$\text{bandwidth (BW)} = f_H - f_L$$

The bandwidth is defined by the lower and upper cutoff frequencies.

- **Cutoff–any frequency at which the gain has dropped by 3 dB.**
- At frequencies above and below the midrange, capacitance and any inductance will affect the gain of the amplifier.

•At low frequencies the coupling and bypass capacitors lower the gain.

•At high frequencies stray capacitances associated with the active device lower the gain.



BJT Amplifier High-Frequency Response
Miller Capacitance:

- **Any *p-n* junction can develop capacitance.**

  In a BJT amplifier, this capacitance becomes noticeable across:

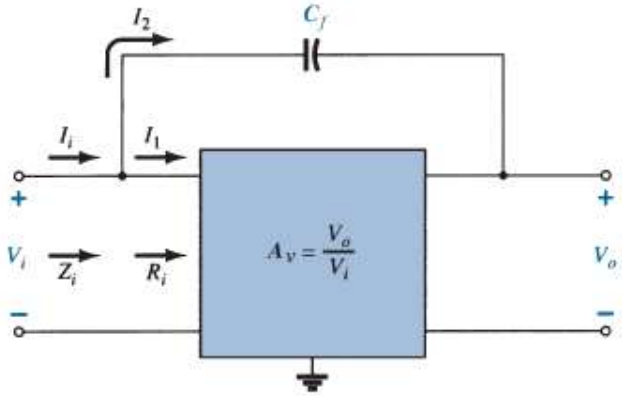
  - **The base-collector junction at high frequencies in common-emitter BJT amplifier configurations**
  - **The gate-drain junction at high frequencies in common-source FET amplifier configurations.**

- **These capacitances are represented as separate input and output capacitances, called the Miller Capacitances.**

Miller input capacitance:

The Miller effect input capacitance is defined by

$$C_{M_i} = (1 - A_v)C_f$$



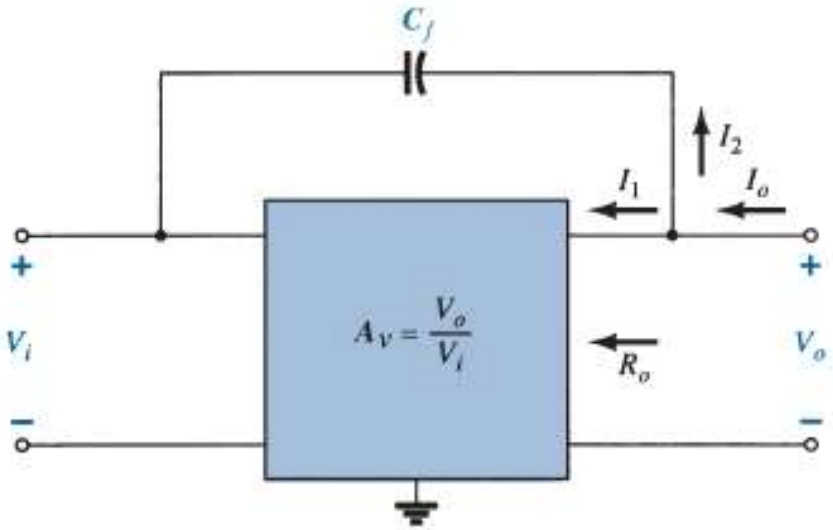
Note that the amount of Miller capacitance is dependent on inter-electrode capacitance from input to output (C_f) and the gain (A_v).

Miller output capacitance:

$$C_{M_o} = \left(1 - \frac{1}{A_v}\right) C_f$$

If the gain (A_v) is considerably greater than 1, then

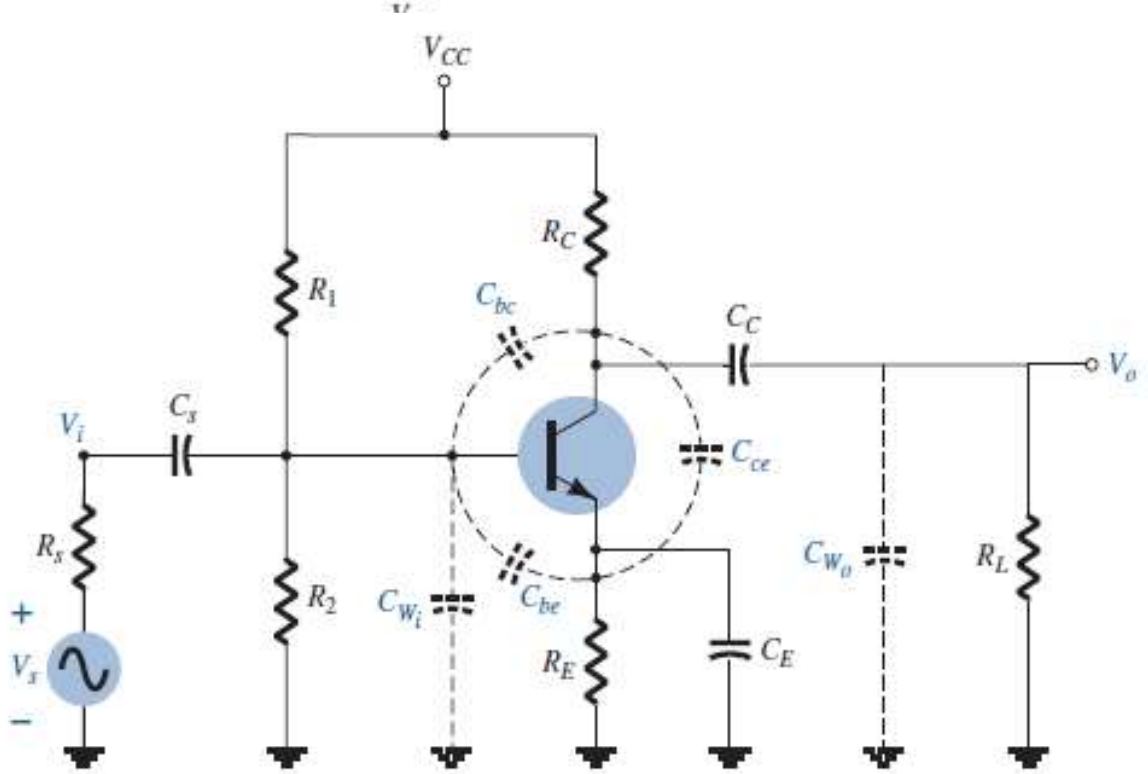
$$C_{M_o} \cong C_f \qquad |A_v| \gg 1$$



BJT Amplifier High-Frequency Response

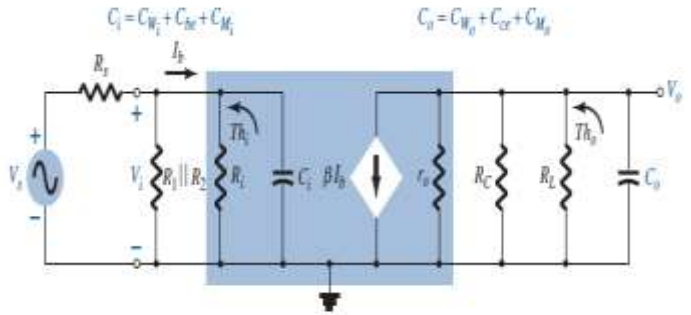
Capacitances that affect the high-frequency response are

- **Junction capacitances**
  C_{be}, C_{bc}, C_{ce}
- **Wiring capacitances**
  C_{wi}, C_{wo}
- Miller capacitance



Network of Fig with the capacitors that affect the high-frequency response.

BJT Amplifier High-Frequency Response:



Input Network (f_{Hi}) High-Frequency Cutoff

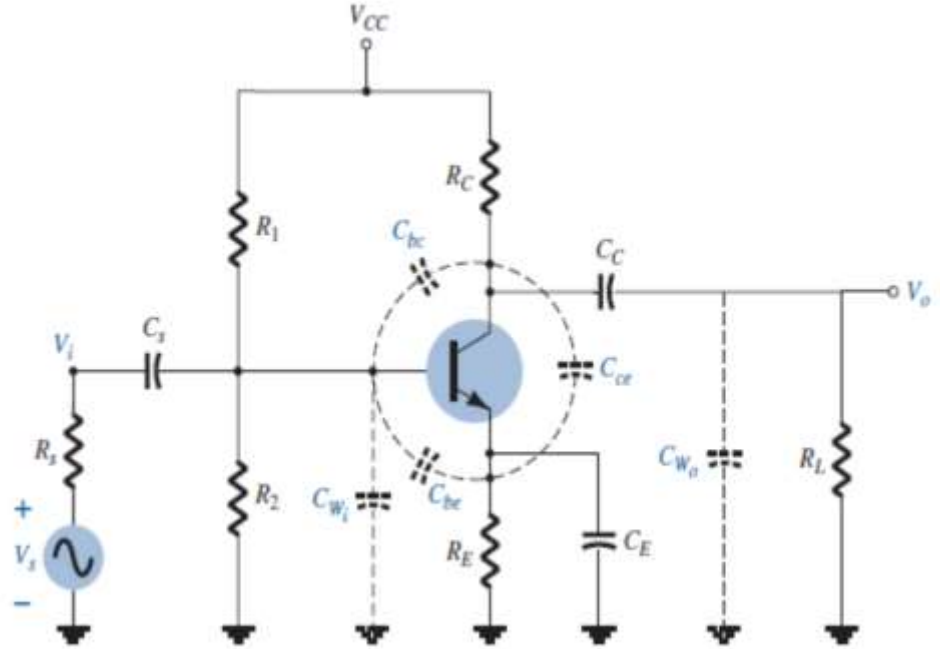
$$f_{Hi} = \frac{1}{2\pi R_{Thi} C_i}$$

where

$$R_{Thi} = R_s \| R_1 \| R_2 \| R_i$$

and

$$C_i = C_{Wi} + C_{be} + C_{Mi}$$
$$= C_{Wi} + C_{be} + (1 - A_v) C_{bc}$$



Output Network (f_{Ho}) High-Frequency Cutoff :

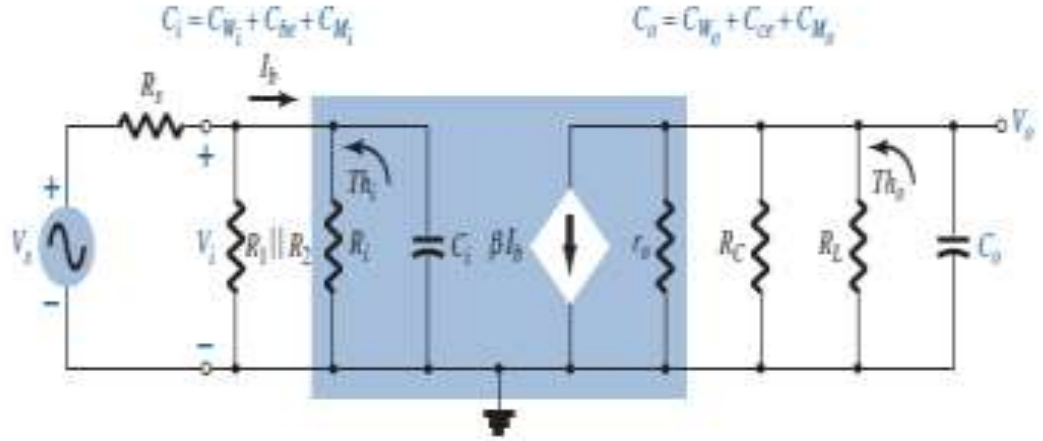
$$f_{Ho} = \frac{1}{2\pi R_{Tho} C_o}$$

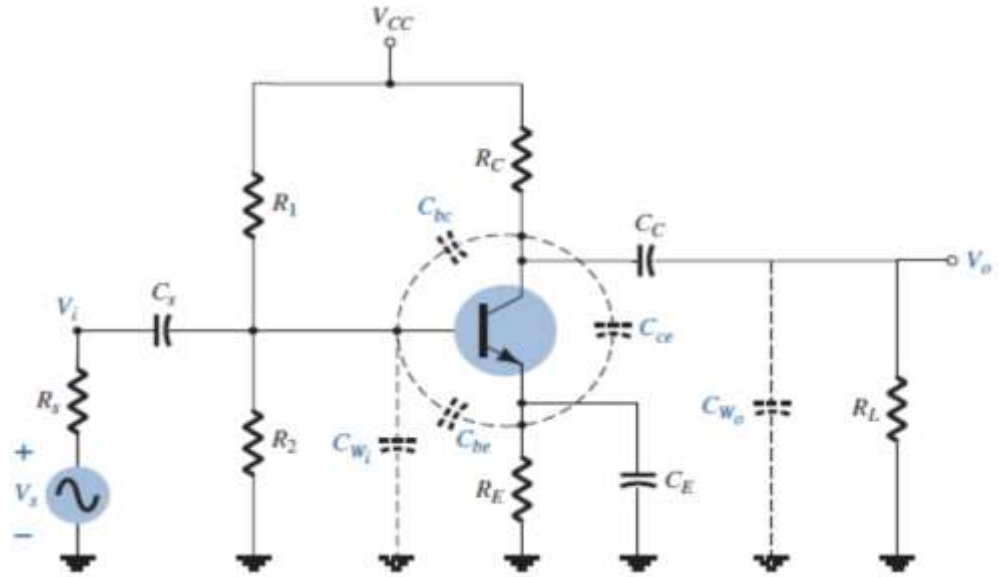
where

$$R_{Tho} = R_C \,||\, R_L \,||\, r_o$$

and

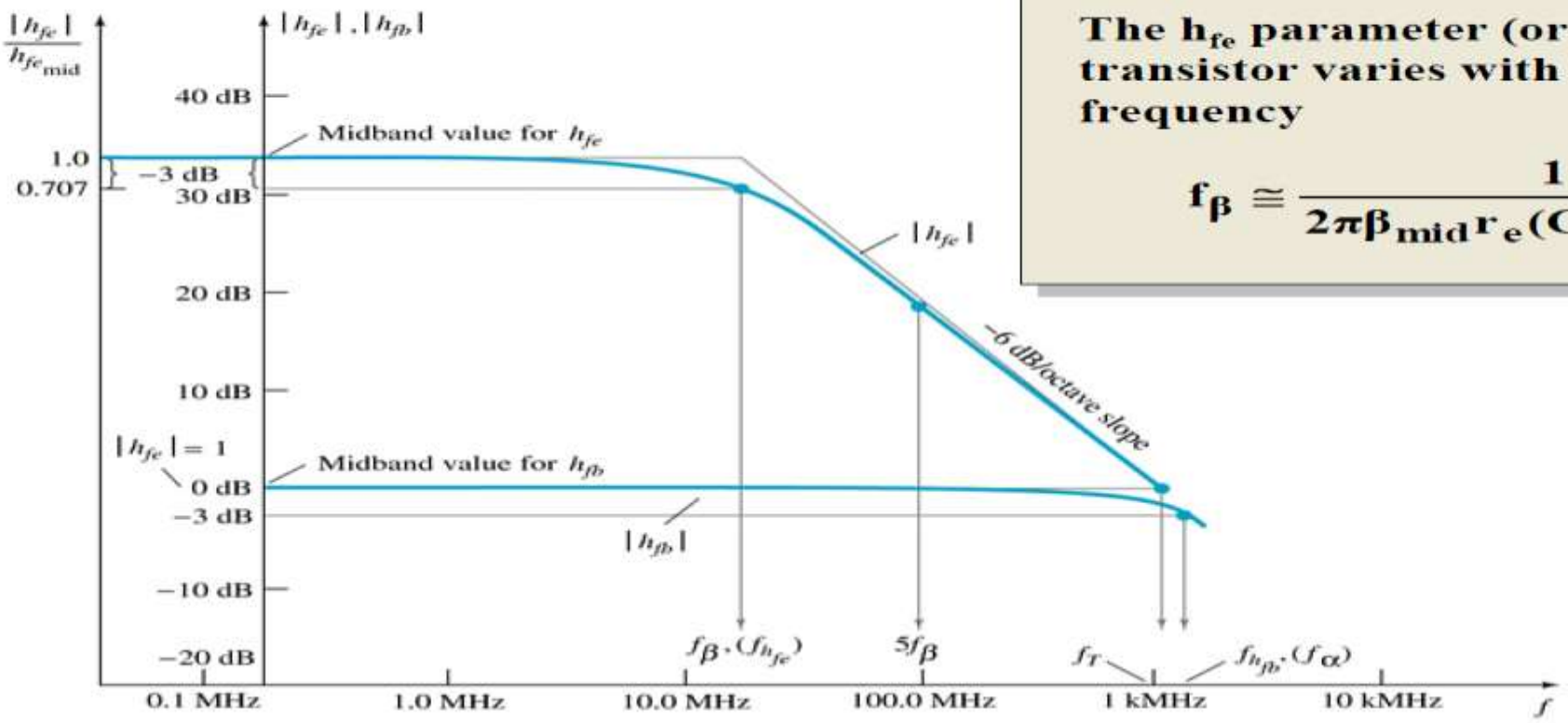
$$C_o = C_{Wo} + C_{ce} + C_{Mo}$$





At the high-frequency end, there are two factors that define the −3-dB cutoff point: the network capacitance (parasitic and introduced) and the frequency dependence of $h_{fe}(\beta)$.

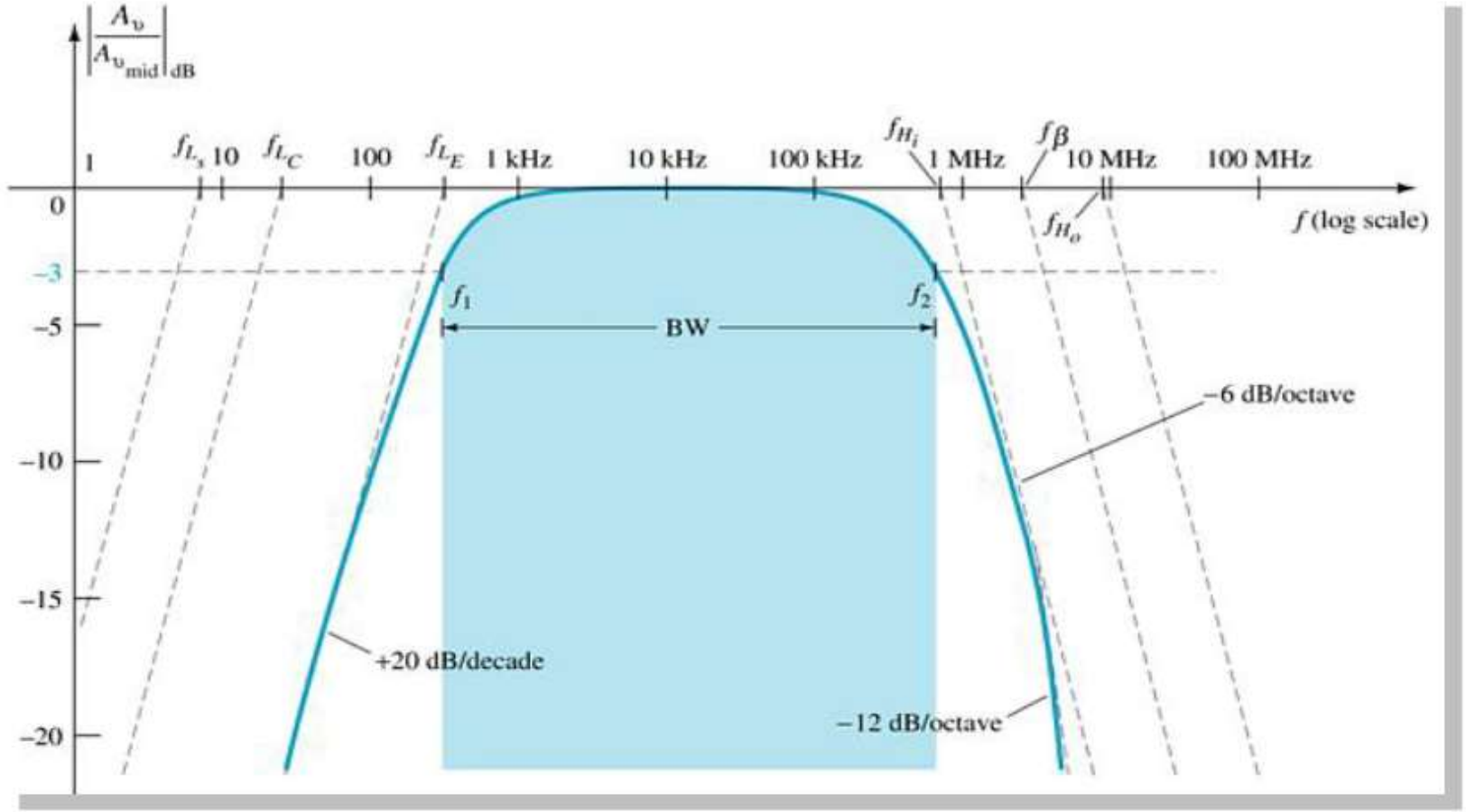
h_{fe} (or β) Variation



The h_{fe} parameter (or β) of a transistor varies with frequency

$$f_{\beta} \cong \frac{1}{2\pi\beta_{mid} r_e (C_{be} + C_{bc})}$$

BJT Amplifier Frequency Response

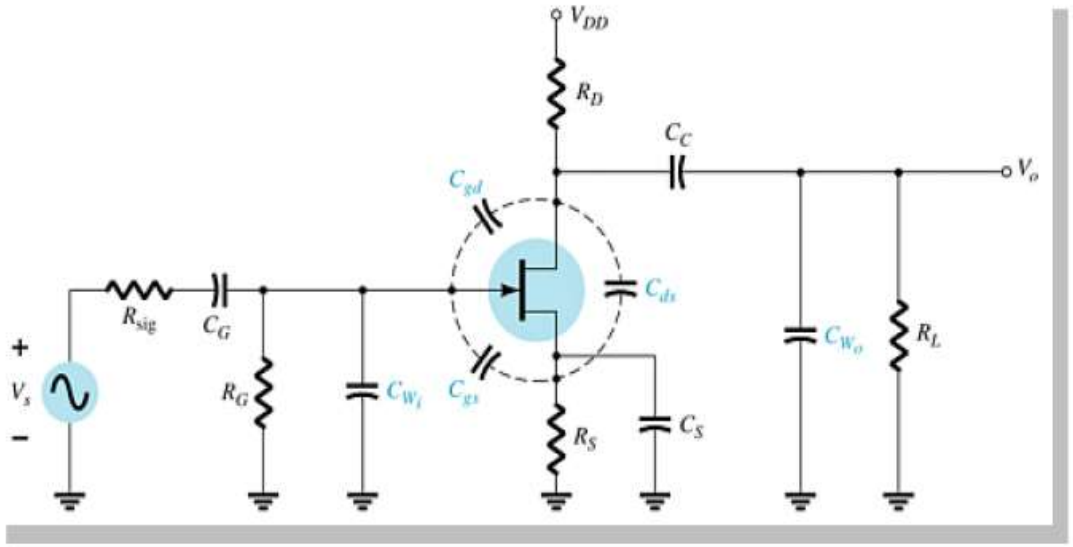


Note the *highest* lower cutoff frequency (f_L) and the *lowest* upper cutoff frequency (f_H) are closest to the actual response of the amplifier.

FET Amplifier High-Frequency Response

Capacitances that affect the high-frequency response are

- **Junction capacitances**
  C_{gs}, C_{gd}, C_{ds}
- **Wiring capacitances**
  C_{wi}, C_{wo}
- Miller capacitances



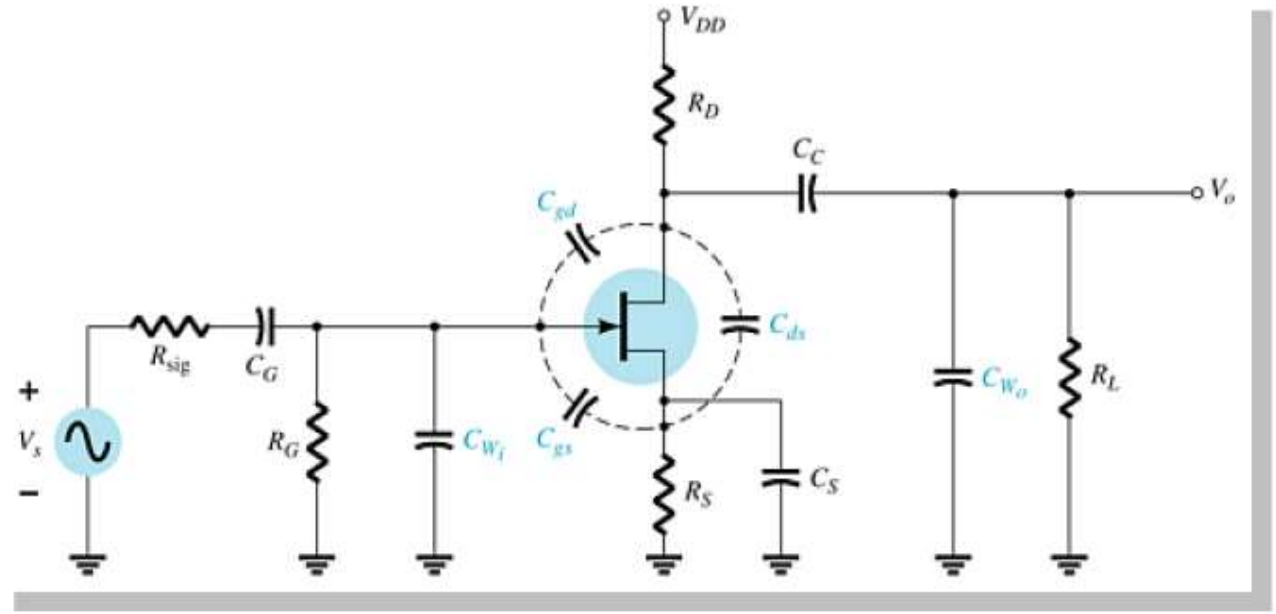
Input Network (f_{Hi}) High-Frequency Cutoff

$$f_{Hi} = \frac{1}{2\pi R_{Thi} C_i}$$

$$C_i = C_{Wi} + C_{gs} + C_{Mi}$$

$$C_{Mi} = (1 - A_v) C_{gd}$$

$$R_{Thi} = R_{sig} \,||\, R_G$$



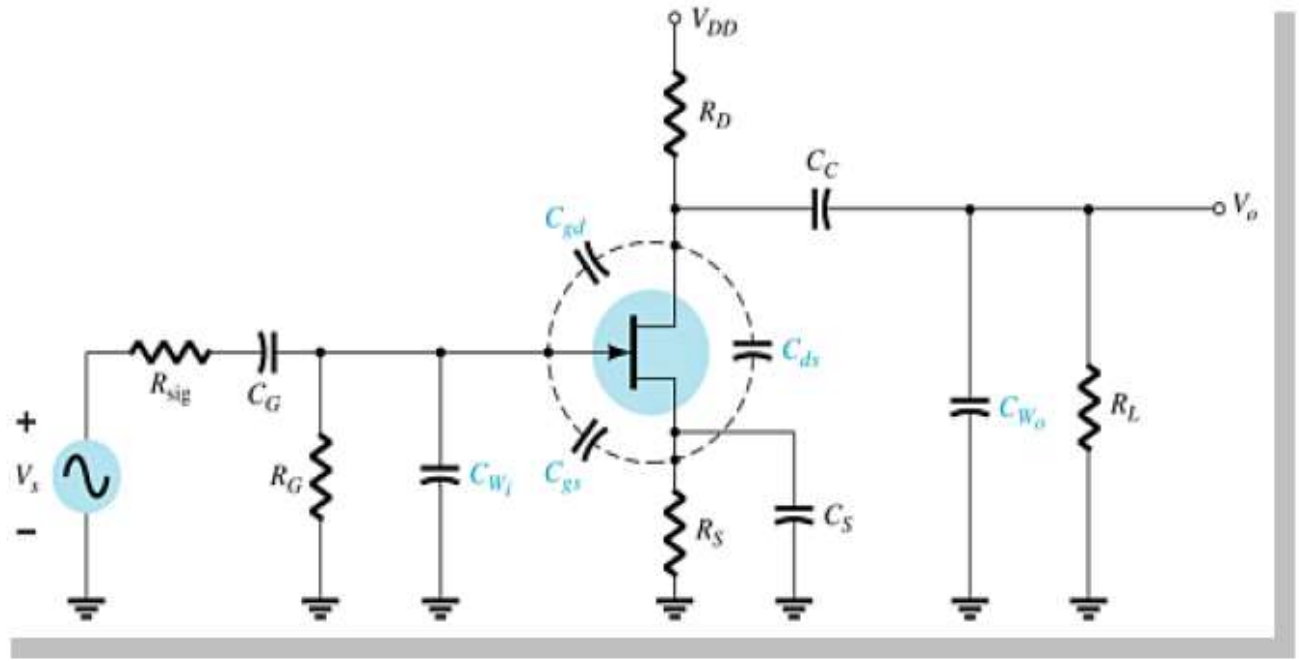
Output Network (f_{Ho}) High-Frequency Cutoff

$$f_{Ho} = \frac{1}{2\pi R_{Tho} C_o}$$

$$C_o = C_{Wo} + C_{ds} + C_{Mo}$$

$$C_{Mo} = \left(1 - \frac{1}{A_v}\right) C_{gd}$$

$$R_{Tho} = R_D \,||\, R_L \,||\, r_d$$



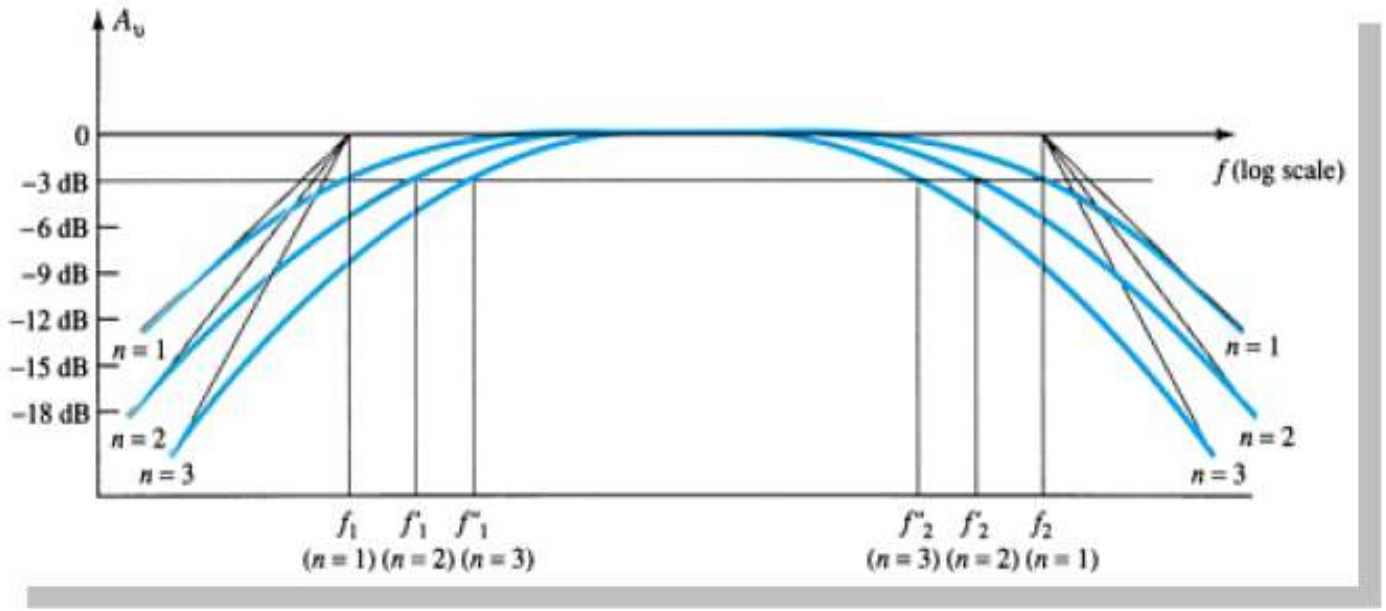
Multistage Frequency Effects:

- **Each stage will have its own frequency response, but the output of one stage will be affected by capacitances in the subsequent stage.**
- **This is especially so when determining the high frequency response. For example, the output capacitance (Co) will be affected by the input Miller Capacitance (C_{Mi}) of the next stage.**

Multistage Amplifier Frequency Response:

$$f_L' = \frac{f_L}{\sqrt{2^{1/n} - 1}}$$

$$f_H' = (\sqrt{2^{1/n} - 1}) f_H$$



Effect of an increased number of stages on the cutoff frequencies and the bandwidth.

Once the cutoff frequencies have been determined for each stage (taking into account the shared capacitances), they can be plotted.

Note the *highest* lower cutoff frequency (f_L) and the *lowest* upper cutoff frequency (f_H) are closest to the actual response of the amplifier.

Classification of Amplifiers

Type of Signal	Type of Configuration	Power Amplifier Classification	Frequency of Operation
Small Signal	Common Emitter	Class A Amplifier	Direct Current (DC)
Large Signal	Common Base	Class B Amplifier	Audio Frequencies (AF)
	Common Collector	Class AB Amplifier	Radio Frequencies (RF)
		Class C Amplifier	VHF, UHF and SHF Frequencies

Classification of Amplifier:

- **Before proceeding with the concept of feedback it is useful to classify amplifiers into 4 basic categories based on their input & output signal relationships.**
  - **Voltage amplifier**
  - **Current amplifier**
  - **Transconductance amplifier**
  - **Transresistance amplifier**

CLASSIFICATION OF AMPLIFIERS

- Voltage Amplifier- An amplifier provides a voltage output proportional to the voltage input and the proportionality factor does not depend on the magnitudes of the source and load resistance
- Current Amplifier- An amplifier which provides an output current proportional to the signal current .

- Transconductance Amplifier- An amplifier in which, the output current is proportional to the signal voltage, independent of the magnitudes of source and load resistance.

- Transresistance Amplifier- An amplifier in which output voltage is proportional to the signal current of the magnitudes of source and load resistance.

FEEDBACK IN AMPLIFIER

FEEDBACK : It is a process in which a portion of the output energy (voltage or current) is transferred to the input of the system. Feedback in amplifier is of two types :

- Positive, Direct or regenerative feedback
- Negative, Inverse or Degenerative feedback

Positive feedback : If the feedback energy is in phase with the input energy, it reinforces or enhances the input signal energy, then it is called positive feedback.

Negative feedback : When the feedback energy is in out of phase (180° phase) with the input energy, it reduces or diminishes the input signal energy, the feedback is called Negative feedback

Classification of Feedback

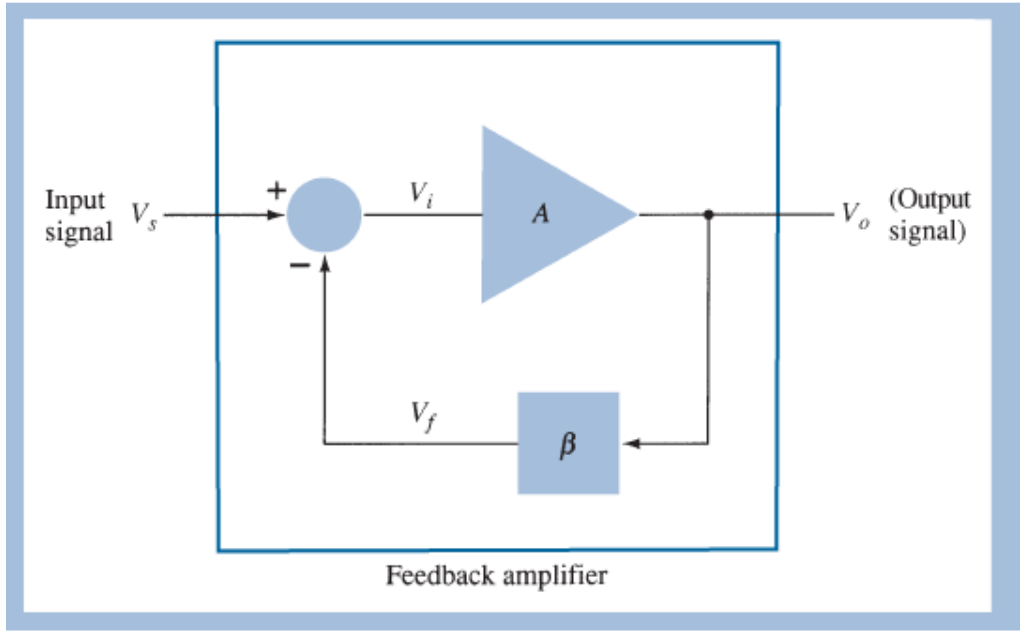
Voltage Feedback : It is the feedback in which the feedback energy is proportional to the output voltage of the amplifier.

Current feedback : It is the feedback in which the feedback energy is proportional to the output current of the amplifier.

Compound feedback : It is the feedback in which the feedback energy is partly proportional to the output voltage of the amplifier and partly proportional to the output current.

Feedback Concept:

A typical feedback connection is shown in Fig.The input signal *Vs* is applied to a mixer network, where it is combined with a feedback signal *Vf*. The difference of these signals *Vi* is then the input voltage to the amplifier. A portion of the amplifier output *Vo* is connected to the feedback network, which provides a reduced portion of the output as feedback signal to the input mixer network.



Negative feedback:

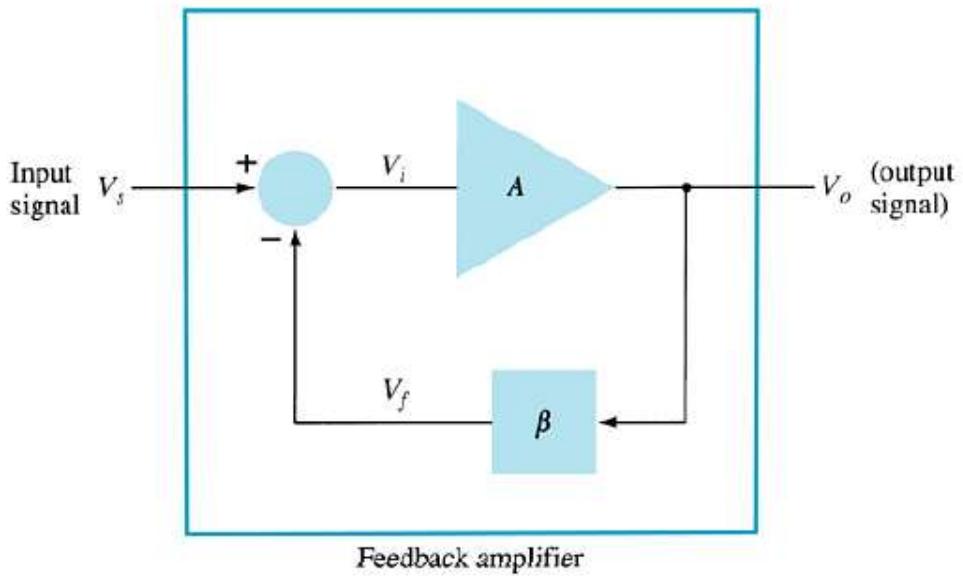
The effects of negative feedback on an amplifier:

Disadvantage

- **Lower gain**

Advantages

- **Higher input impedance**
- **More stable gain**
- **Improved frequency response**
- **Lower output impedance**
- **Reduced noise**
- **More linear operation**



Feedback amplifier

Contents of the Class:

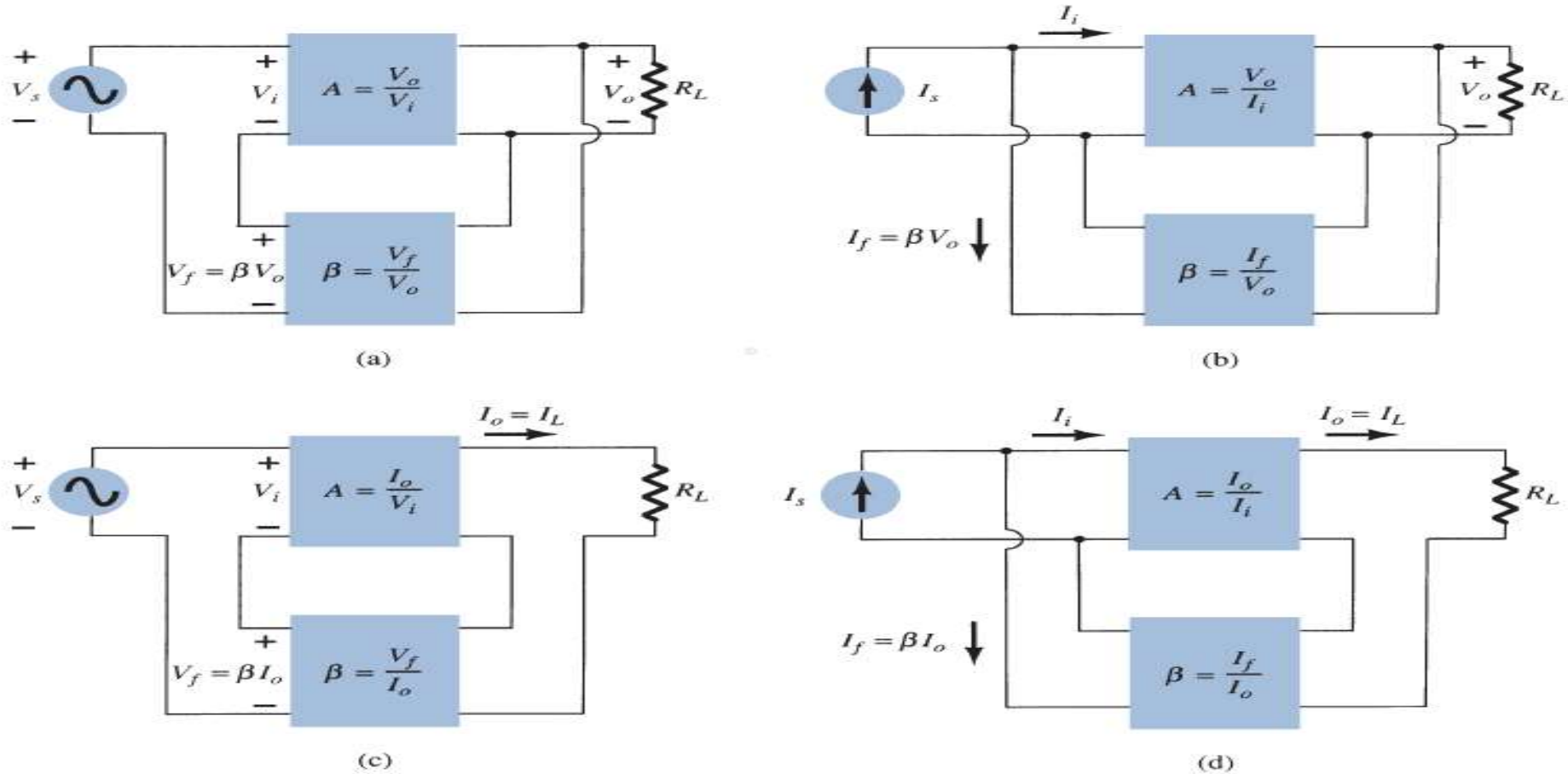
- Feedback Connection Types
- Voltage series feedback
- Current series feedback
- Voltage shunt feedback
- Current shunt feedback
- Transfer gain
- Input-output resistance or impedence

- Referred Book:- R L Boylestad

Feedback Connection Types:

- There are four basic ways of connecting the feedback signal. Both *voltage* and *current* can be fed back to the input either in *series* or *parallel.* Specifically, there can be:

1. Voltage-series feedback
2. Voltage-shunt feedback
3. Current-series feedback
4. Current-shunt feedback



Feedback amplifier types: (a) voltage-series feedback, $A_f = V_o/V_s$; (b) voltage-shunt feedback, $A_f = V_o/I_s$; (c) current-series feedback, $A_f = I_o/V_s$; (d) current-shunt feedback, $A_f = I_o/I_s$.

In the list above, *voltage* refers to connecting the output voltage as input to the feedback network; *current* refers to tapping off some output current through the feedback network. *Series* refers to connecting the feedback signal in series with the input signal voltage; *shunt* refers to connecting the feedback signal in shunt (parallel) with an input current source.

Series feedback connections tend to *increase* the input resistance, whereas shunt feedback connections tend to *decrease* the input resistance.

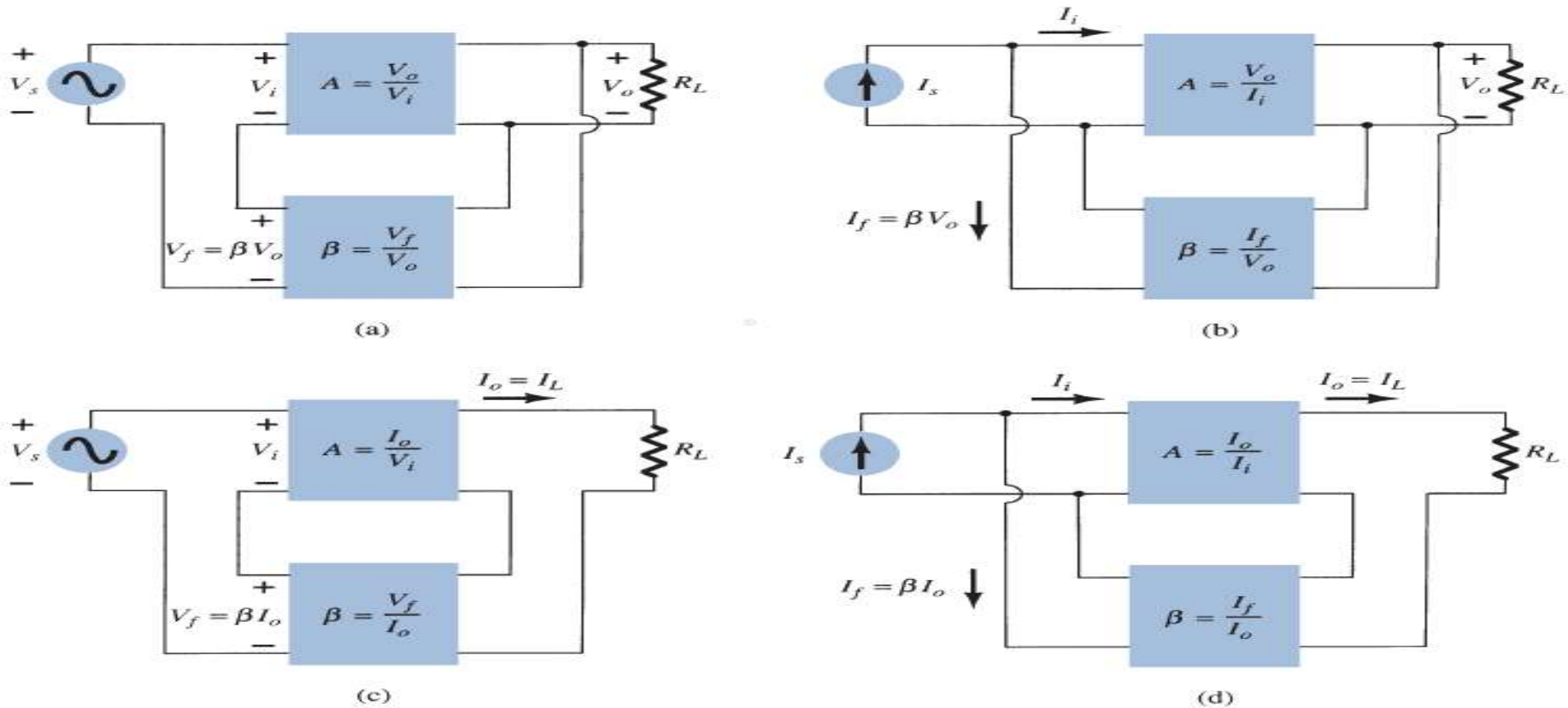
Voltage feedback tends to *decrease* the output impedance, whereas current feedback tends to *increase* the output impedance. Typically, higher input and lower output impedances are desired for most cascade amplifiers.

Both of these are provided using the voltage-series feedback connection.
We shall therefore concentrate first on this amplifier connection.

Gain with Feedback

The gain without feedback, A, is that of the amplifier stage. With feedback β, the overall gain of the circuit is reduced by a factor $(1 + \beta A)$.

		Voltage-Series	Voltage-Shunt	Current-Series	Current-Shunt
Gain without feedback	A	$\frac{V_o}{V_i}$	$\frac{V_o}{I_i}$	$\frac{I_o}{V_i}$	$\frac{I_o}{I_i}$
Feedback	β	$\frac{V_f}{V_o}$	$\frac{I_f}{V_o}$	$\frac{V_f}{I_o}$	$\frac{I_f}{I_o}$
Gain with feedback	A_f	$\frac{V_o}{V_s}$	$\frac{V_o}{I_s}$	$\frac{I_o}{V_s}$	$\frac{I_o}{I_s}$



Feedback amplifier types: (a) voltage-series feedback, $A_f = V_o/V_s$; (b) voltage-shunt feedback, $A_f = V_o/I_s$; (c) current-series feedback, $A_f = I_o/V_s$; (d) current-shunt feedback, $A_f = I_o/I_s$.

Voltage-Series Feedback Figure shows the voltage-series feedback connection with a part of the output voltage fed back in series with the input signal, resulting in an overall gain reduction. If there is no feedback ($V_f = 0$), the voltage gain of the amplifier stage is

$$A = \frac{V_o}{V_s} = \frac{V_o}{V_i}$$

If a feedback signal V_f is connected in series with the input, then

$$V_i = V_s - V_f$$

Since $$V_o = AV_i = A(V_s - V_f) = AV_s - AV_f = AV_s - A(\beta V_o)$$

then $$(1 + \beta A)V_o = AV_s$$

so that the overall voltage gain *with* feedback is

$$\boxed{A_f = \frac{V_o}{V_s} = \frac{A}{1 + \beta A}}$$

Equation shows that the gain *with* feedback is the amplifier gain reduced by the factor $(1 + \beta A)$. This factor will be seen also to affect input and output impedance among other circuit features.

Voltage-Shunt Feedback The gain with feedback for the network of Fig. is

$$A_f = \frac{V_o}{I_s} = \frac{A\,I_i}{I_i + I_f} = \frac{A\,I_i}{I_i + \beta V_o} = \frac{A\,I_i}{I_i + \beta A\,I_i}$$

$$\boxed{A_f = \frac{A}{1 + \beta A}}$$

Input Impedance with Feedback:

Voltage-Series Feedback A more detailed voltage-series feedback connection is shown in Fig. The input impedance can be determined as follows:

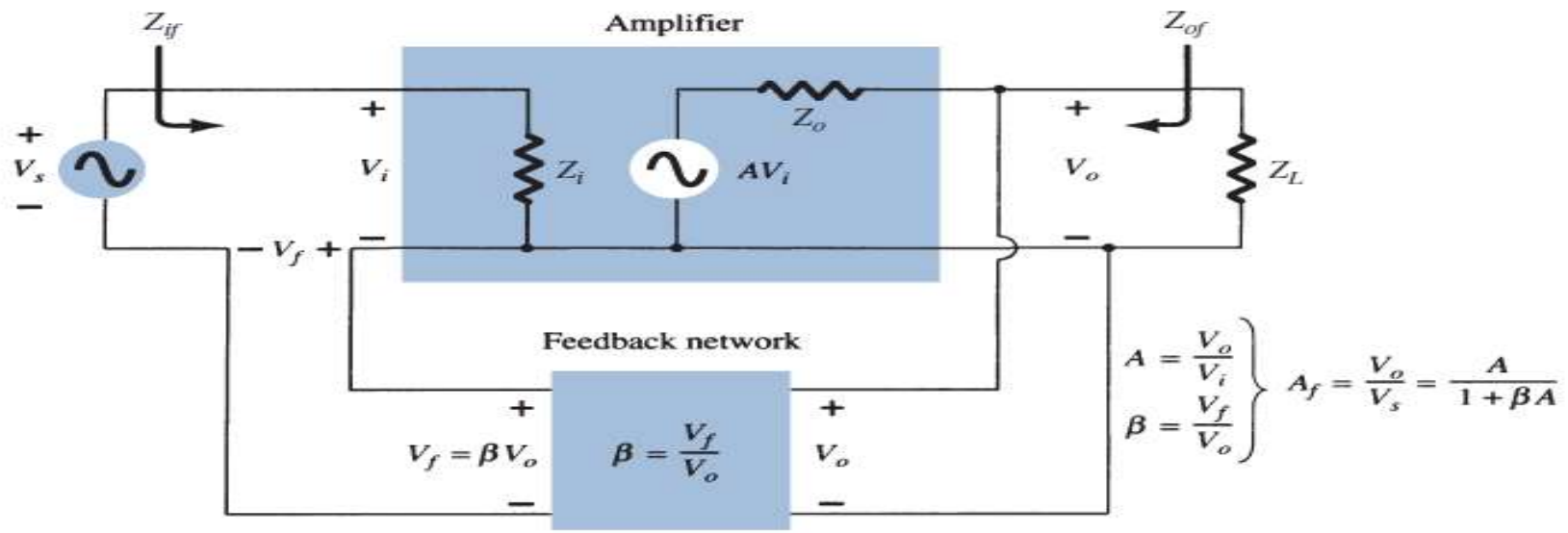
$$I_i = \frac{V_i}{Z_i} = \frac{V_s - V_f}{Z_i} = \frac{V_s - \beta V_o}{Z_i} = \frac{V_s - \beta A V_i}{Z_i}$$

$$I_i Z_i = V_s - \beta A V_i$$

$$V_s = I_i Z_i + \beta A V_i = I_i Z_i + \beta A I_i Z_i$$

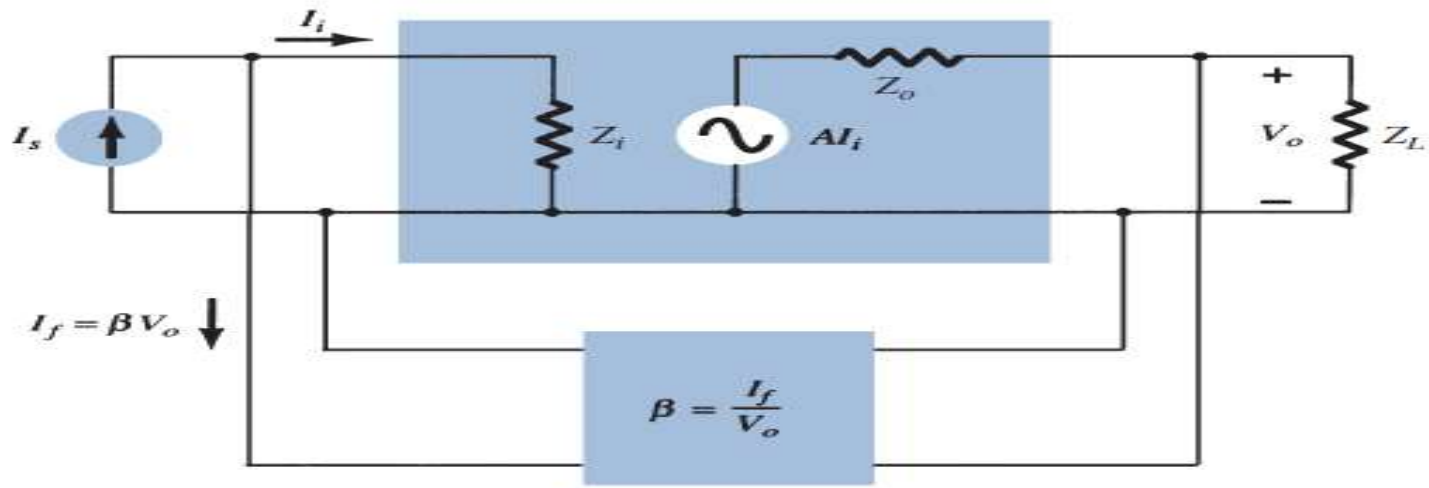
$$\boxed{Z_{if} = \frac{V_s}{I_i} = Z_i + (\beta A) Z_i = Z_i(1 + \beta A)}$$

The input impedance with series feedback is seen to be the value of the input impedance without feedback multiplied by the factor $(1 + \beta A)$, and applies to both voltage-series and current-series configurations.



Voltage-series feedback connection.

Voltage-Shunt Feedback A more detailed voltage-shunt feedback connection is shown in Fig. The input impedance can be determined to be



Voltage-shunt feedback connection.

$$Z_{if} = \frac{V_i}{I_s} = \frac{V_i}{I_i + I_f} = \frac{V_i}{I_i + \beta V_o}$$

$$= \frac{V_i/I_i}{I_i/I_i + \beta V_o/I_i}$$

$$\boxed{Z_{if} = \frac{Z_i}{1 + \beta A}}$$

Output impedance with Feedback:

Voltage-Series Feedback The voltage-series feedback circuit of Fig. provides sufficient circuit detail to determine the output impedance with feedback. The output impedance is determined by applying a voltage V, resulting in a current I, with V_s shorted out ($V_s = 0$). The voltage V is then

$$V = IZ_o + AV_i$$

For $V_s = 0$, $V_i = -V_f$

so that $V = IZ_o - AV_f = IZ_o - A(\beta V)$

Rewriting the equation as

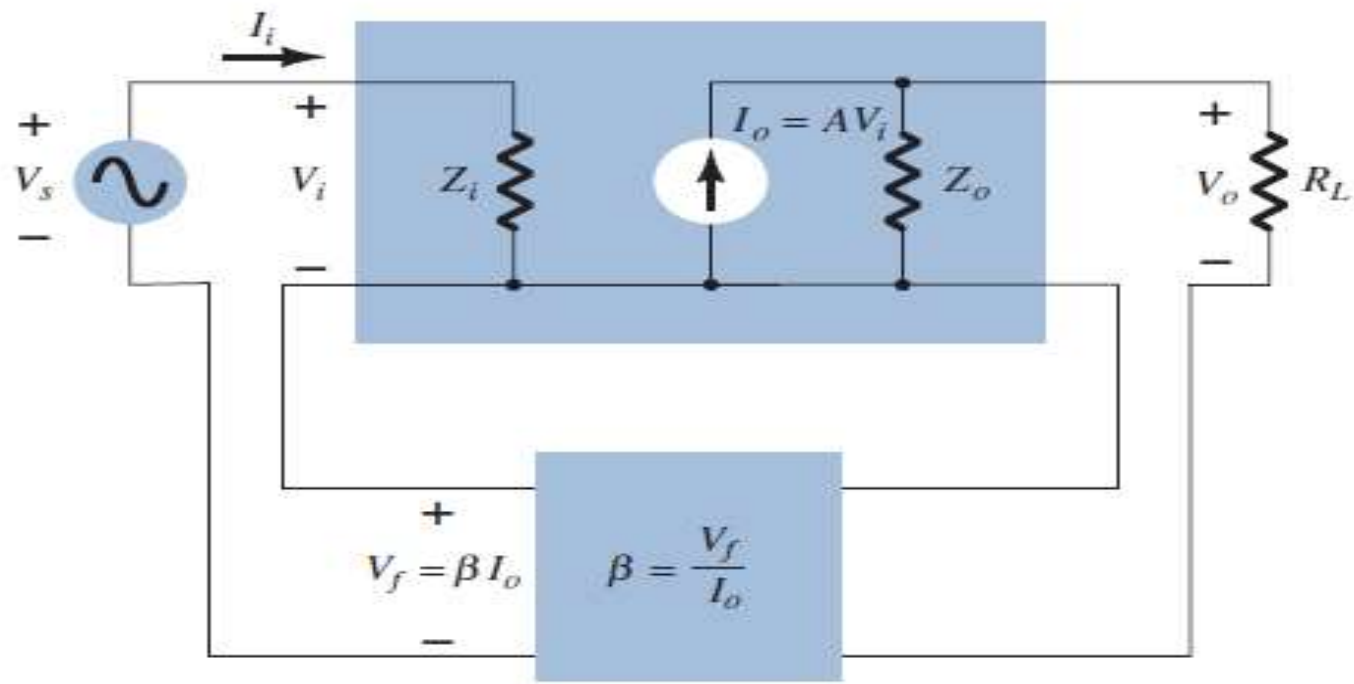
$$V + \beta AV = IZ_o$$

allows solving for the output impedance with feedback:

$$Z_{of} = \frac{V}{I} = \frac{Z_o}{1 + \beta A}$$

Equation shows that with voltage-series feedback the output impedance is reduced from that without feedback by the factor $(1 + \beta A)$.

Current-Series Feedback The output impedance with current-series feedback can be determined by applying a signal V to the output with V_s shorted out, resulting in a current I, the ratio of V to I being the output impedance. Figure shows a more detailed



Current-series feedback connection.

connection with current-series feedback. For the output part of a current-series feedback connection shown in Fig. the resulting output impedance is determined as follows. With $V_s = 0$,

$$V_i = V_f$$

$$I = \frac{V}{Z_o} - AV_i = \frac{V}{Z_o} - AV_f = \frac{V}{Z_o} - A\beta I$$

$$Z_o(1 + \beta A)I = V$$

$$\boxed{Z_{of} = \frac{V}{I} = Z_o(1 + \beta A)}$$

summary

Effect of Feedback Connection on Input and Output Impedance

Voltage-Series	Current-Series	Voltage-Shunt	Current-Shunt
Z_{if} $Z_i(1 + \beta A)$ (increased)	$Z_i(1 + \beta A)$ (increased)	$\frac{Z_i}{1 + \beta A}$ (decreased)	$\frac{Z_i}{1 + \beta A}$ (decreased)
Z_{of} $\frac{Z_o}{1 + \beta A}$ (decreased)	$Z_o(1 + \beta A)$ (increased)	$\frac{Z_o}{1 + \beta A}$ (decreased)	$Z_o(1 + \beta A)$ (increased)

Frequency Distortion with Feedback:

If the feedback network is purely resistive, then the gain with feedback will be less dependent on frequency variations. In some cases the resistive feedback removes all dependence on frequency variations.

• If the feedback includes frequency dependent components (capacitors and inductors), then the frequency response of the amplifier will be affected.

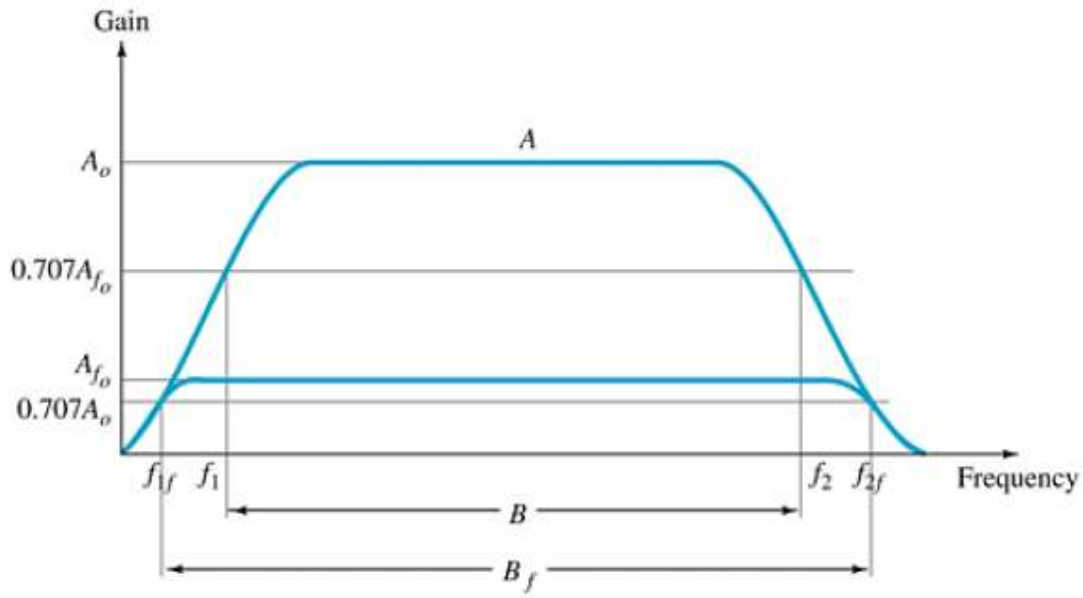
Noise and Nonlinear Distortion:

The feedback network reduces noise by cancellation. The phase of the feedback signal is often opposite the phase of the input signal.

• Nonlinear distortion is also reduced simply because the gain is reduced. The amplifier is operating in midrange and not at the extremes.

Bandwidth with Feedback:

Feedback increases the bandwidth of an amplifier.



Gain Stability with Feedback:

Gain calculations with feedback are often based on external resistive elements in the circuit. By removing gain calculations from internal variations of β and g_m, the gain becomes more stable.

Phase and Frequency Considerations:

At higher frequencies the feedback signal may no longer be out of phase with the input. The feedback is thus positive and the amplifier, itself, becomes unstable

Practical Feedback Circuits:

Voltage-series Feedback:

$$A = \frac{V_o}{V_i} = -g_m R_L$$

where R_L is the parallel combination of resistors:

$$R_L = R_D R_o (R_1 + R_2)$$

The feedback network provides a feedback factor of

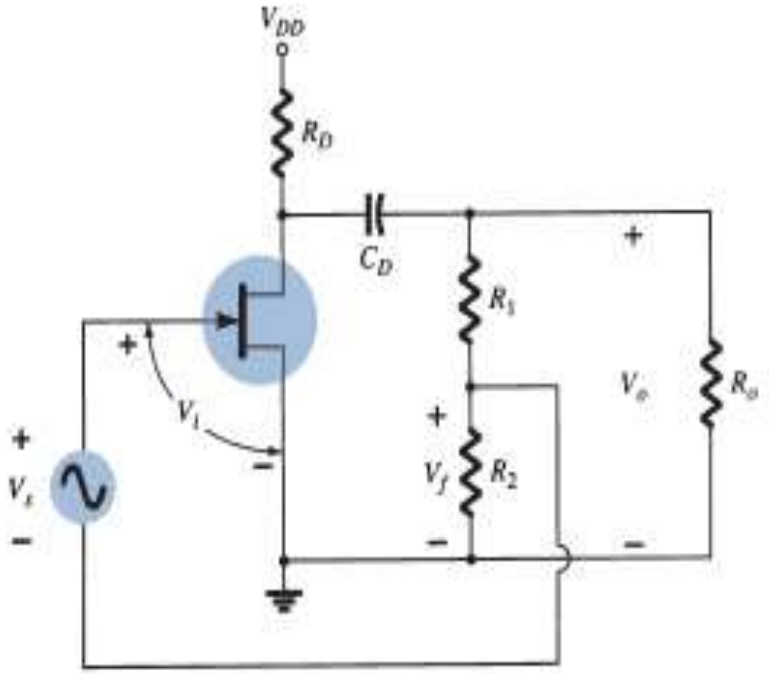
$$\beta = \frac{V_f}{V_o} = \frac{-R_2}{R_1 + R_2}$$

$$A_f = \frac{A}{1 + \beta A} = \frac{-g_m R_L}{1 + [R_2 R_L/(R_1 + R_2)]g_m}$$

If $\beta A \gg 1$, we have

$$A_f \cong \frac{1}{\beta} = -\frac{R_1 + R_2}{R_2}$$

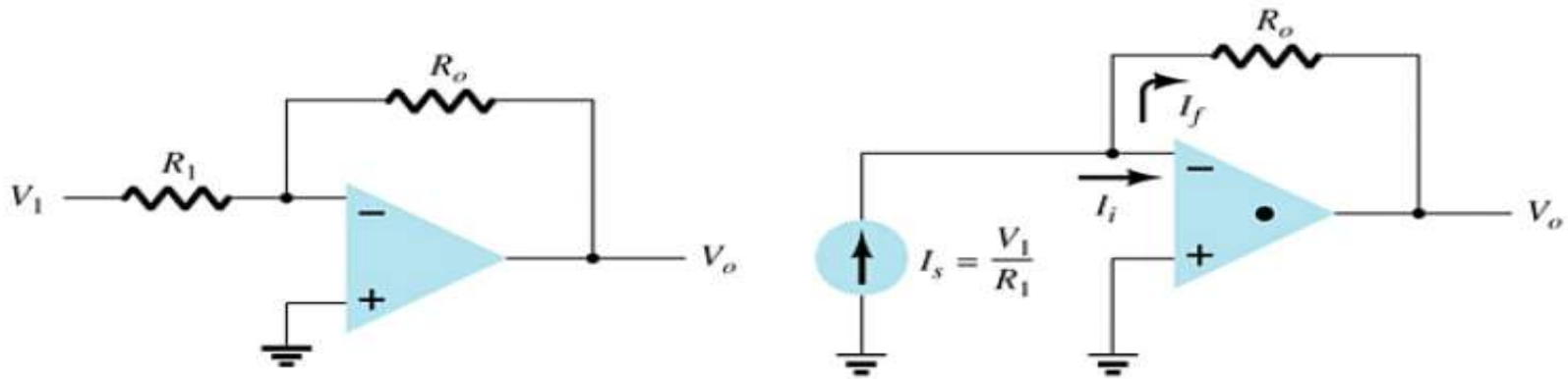
$$A = \frac{V_o}{V_i} = -g_m R_L$$



FET amplifier stage with voltage-series feedback.

Voltage-Shunt Feedback

For a voltage-shunt feedback amplifier, the output voltage is fed back in parallel with the input.

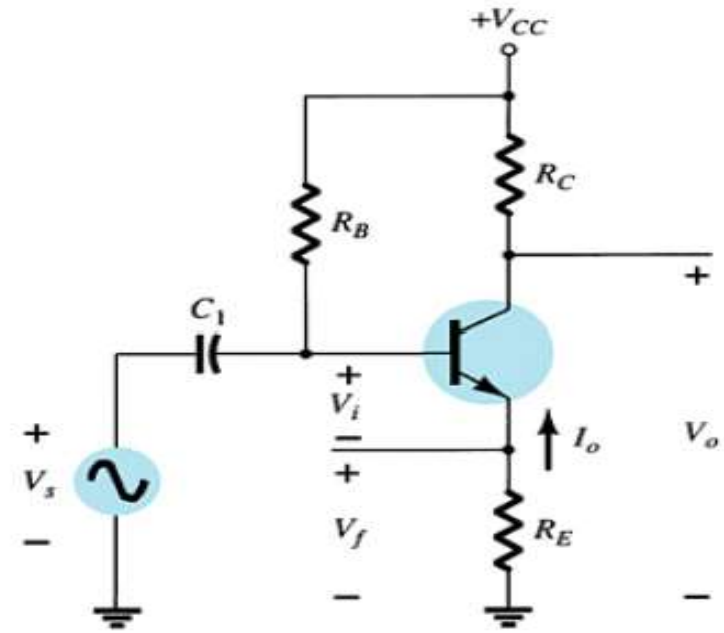


The feedback gain is given by

$$\mathbf{A_f = -\frac{R_o}{R_i}}$$

Current-Series Feedback

For a current-series feedback amplifier, a portion of the output current is fed back in series with the input.

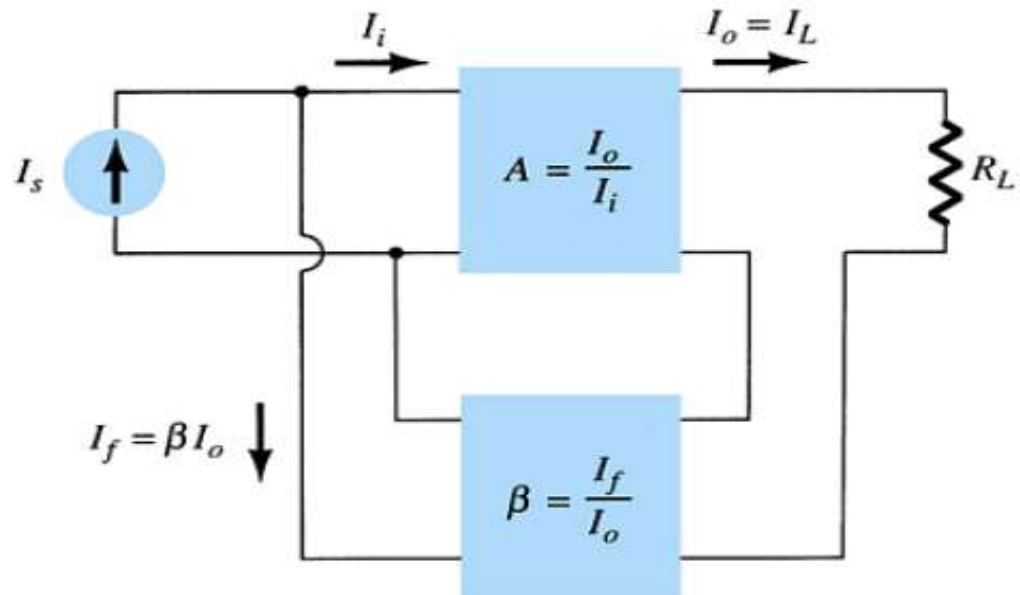


To determine the feedback gain:

$$A_f = \frac{I_o}{V_s} = \frac{A}{1+\beta A} = \frac{-h_{fe}/h_{ie}}{1+(-R_E)\left(\dfrac{-h_{fe}}{h_{ie}+R_E}\right)} \cong \frac{-h_{fe}}{h_{ie}+h_{fe}R_E}$$

Current-Shunt Feedback

For a current-shunt feedback amplifier, a portion of the output current is directed back in parallel with the input.



The feedback gain is given by:

$$\mathbf{A_f = \frac{I_o}{I_s}}$$

Contents of the Class:

- The basic operational amplifier (OPAMP)
- Inverting Amplifier
- Non Inverting Amplifier
- Unit Follower
- Summing Amplifier

- Referred Book:- R L Boylestad

Operational Amplifiers:

- An operational amplifier, or op-amp, is a very high gain differential amplifier with high input impedance and low output impedance. Typical uses of the operational amplifier are to provide voltage amplitude changes (amplitude and polarity), oscillators, filter circuits, and many types of instrumentation circuits. An op-amp contains a number of differential amplifier stages to achieve a very high voltage gain.

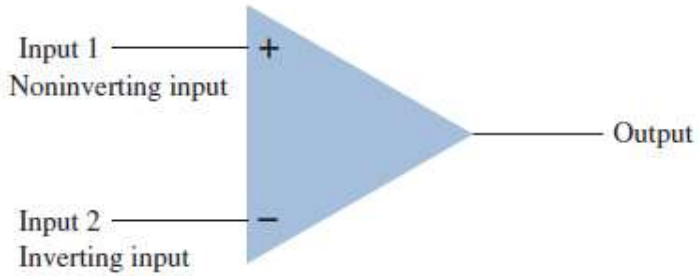


FIG. 1
Basic op-amp.

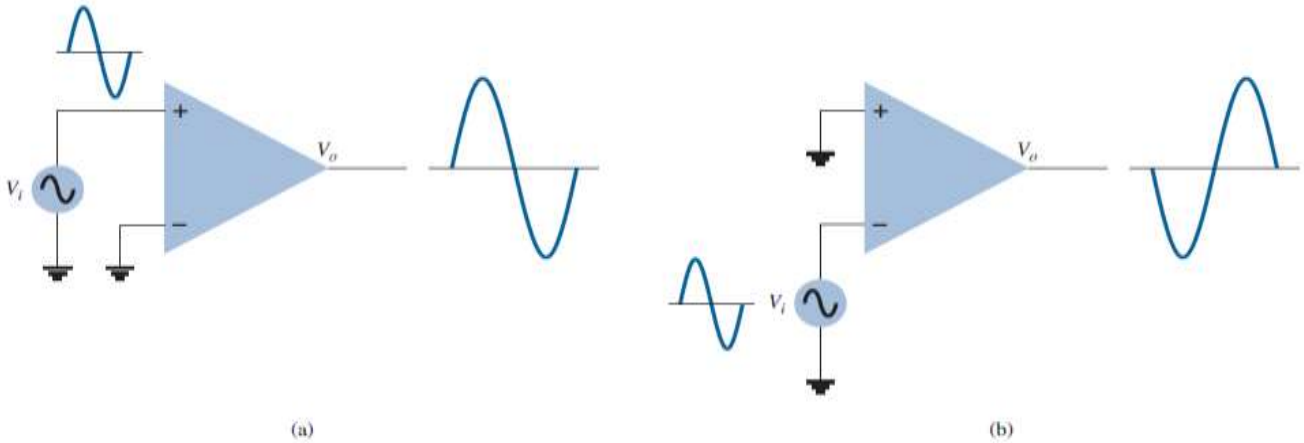


FIG. 2
Single-ended operation.

Single-ended input operation results when the input signal is connected to one input with the other input connected to ground.

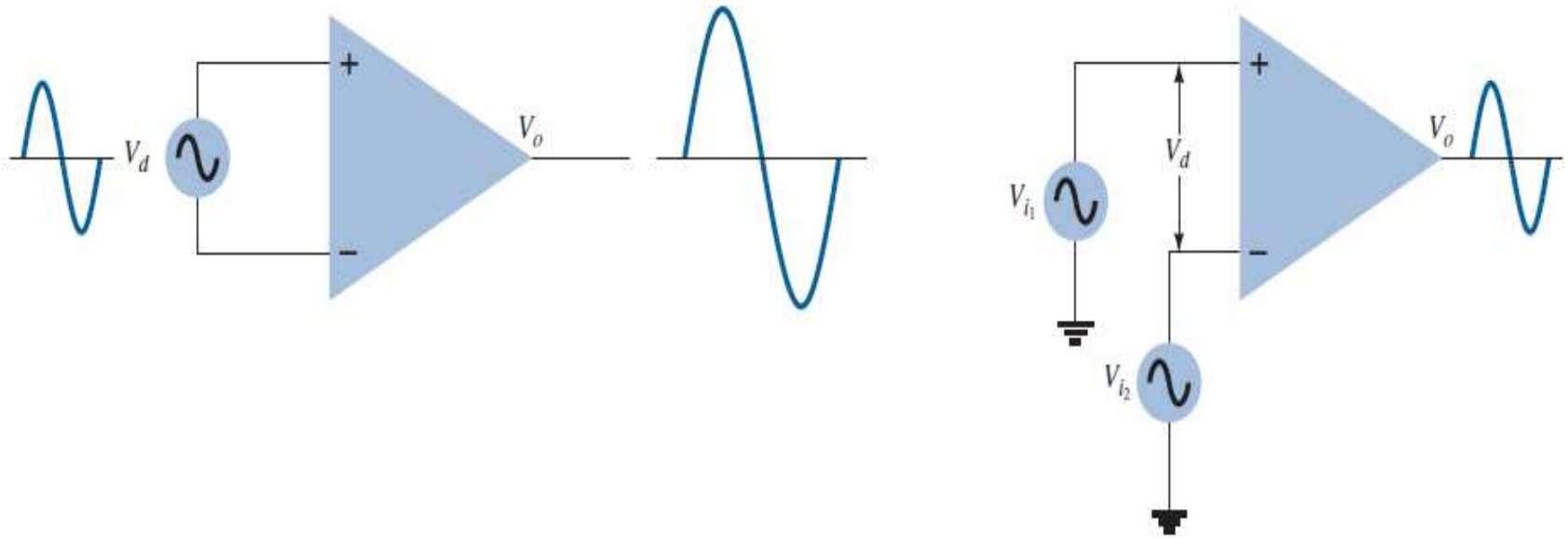


FIG. 3
Double-ended (differential) operation.

In addition to using only one input, it is possible to apply signals at each input—this being a double-ended operation.

when two separate signals are applied to the inputs, the difference signal being V_{i1} - V_{i2}. is amplified.

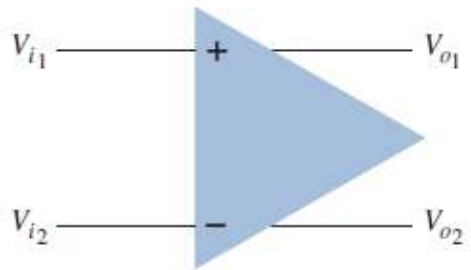


FIG. 4
Double-ended input with double-ended output.

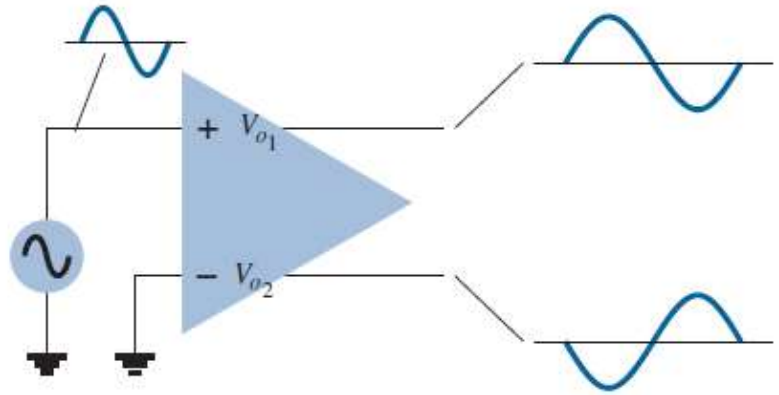


FIG. 5
Single-ended input with double-ended output.

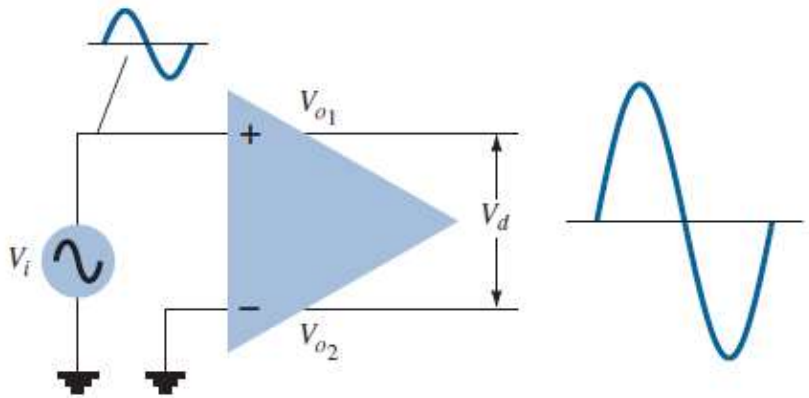


FIG. 6
Differential-output.

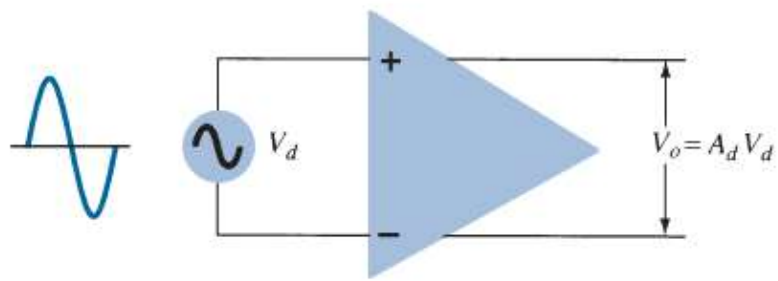


FIG. 7
Differential-input, differential-output operation.

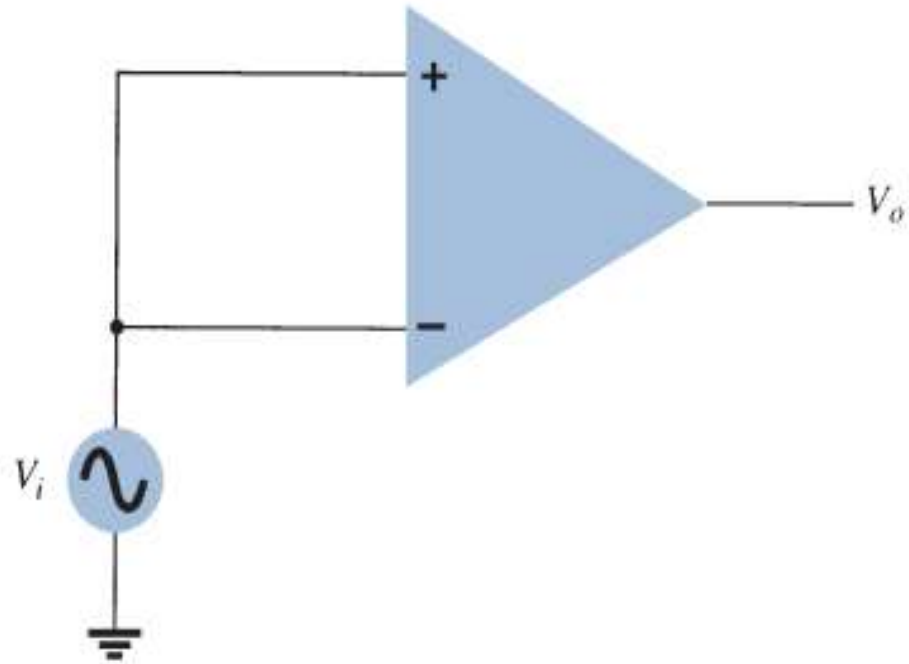


FIG. 8
Common-mode operation.

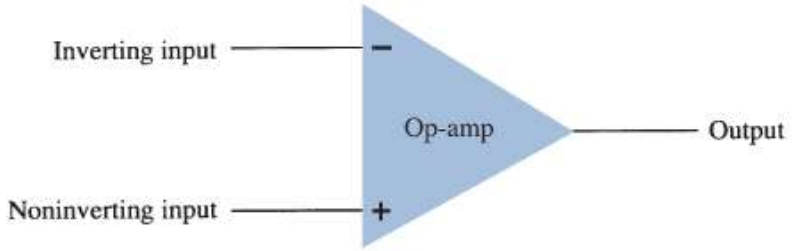
When the same input signals are applied to both inputs, common-mode operation results, Ideally, the two inputs are equally amplified, and since they result in opposite-polarity signals at the output, these signals cancel, resulting in 0-V output. Practically, a small output signal will result.

Common-Mode rejection

A significant feature of a differential connection is that the signals that are opposite at the inputs are highly amplified, whereas those that are common to the two inputs are only slightly amplified—the overall operation being to amplify the difference signal while rejecting the common signal at the two inputs. Since noise (any unwanted input signal) is generally common to both inputs, the differential connection tends to provide attenuation of this unwanted input while providing an amplified output of the difference signal applied to the inputs. This operating feature is referred to as *common-mode rejection*.

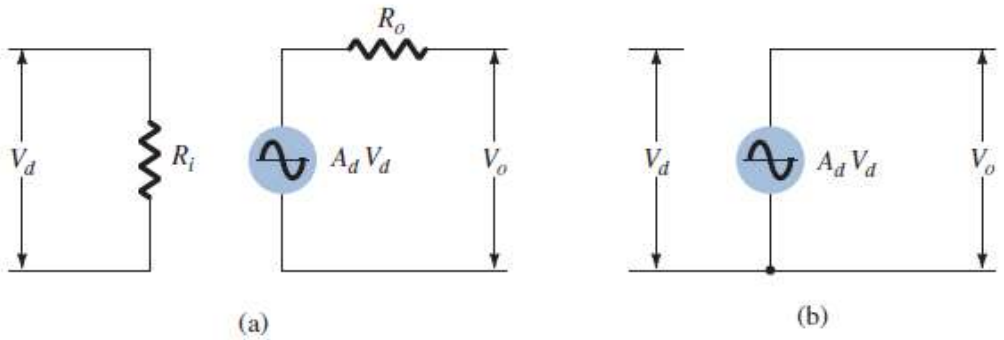
OP-AMP Basics:

An operational amplifier is a very high gain amplifier having very high input impedance (typically a few megohms) and low output impedance (less than 100 ohms). The basic circuit
is made using a difference amplifier having two inputs (plus and minus) and at least one output. As discussed earlier, the plus (1) input produces an output that is in phase with the signal applied, whereas an input to the minus (2) input results in an opposite-polarity output.



Basic op-amp.

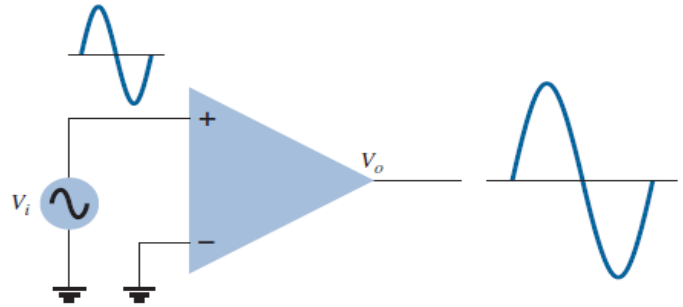
The ac equivalent circuit of the op-amp is shown in Fig. As shown, the input signal applied between input terminals sees an input impedance *Ri* that is typically very high. The output voltage is shown to be the amplifier gain times the input signal taken through an output impedance *Ro*, which is typically very low. An ideal op-amp circuit, as shown in Fig. would have infinite input impedance, zero output impedance, and infinite voltage gain.



AC equivalent of op-amp circuit: (a) practical; (b) ideal.

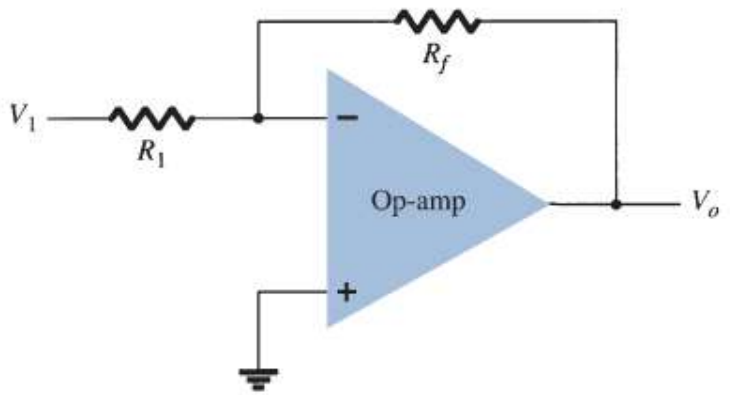
Op-Amp Gain:

Op-Amps have a very high gain. They can be connected open-loop or closed-loop.



• Open-loop refers to a configuration where there is no feedback from output back to the input. In the open-loop configuration the gain can exceed 10,000.

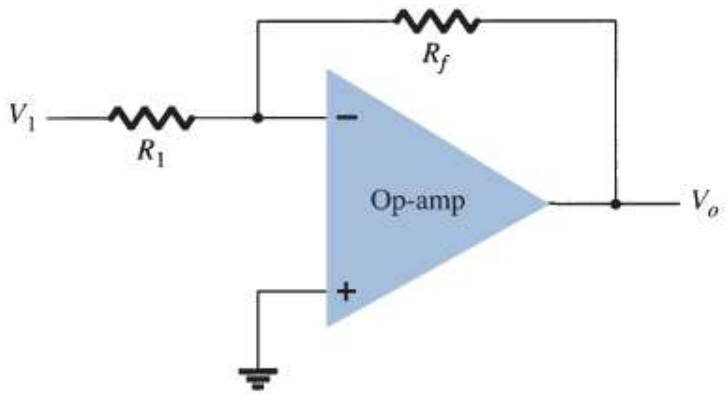
• Closed-loop configuration reduces the gain. In order to control the gain of an op-amp it must have feedback. This feedback is a negative feedback. A negative feedback reduces the gain and improves many characteristics of the op-amp.



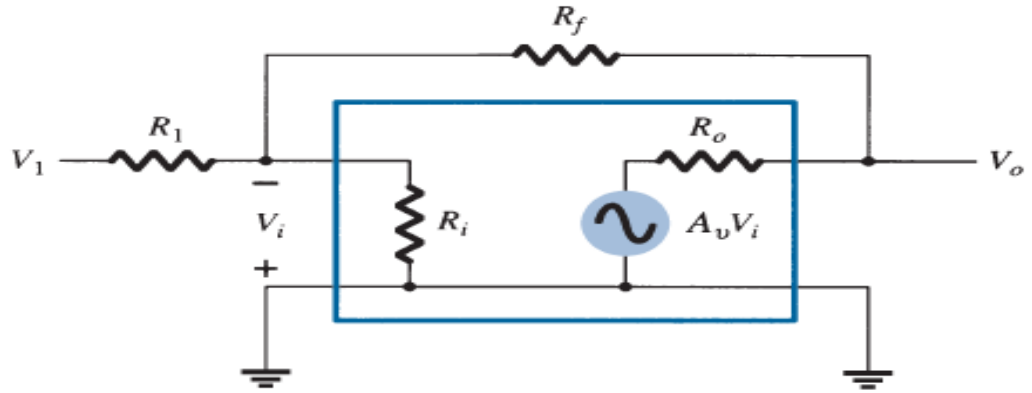
Inverting Op-Amp:

- The basic circuit connection using an op-amp is shown in Fig. The circuit shown provides operation as a constant-gain multiplier. An input signal *V*1 is applied through resistor *R*1 to the minus input.
- The output is then connected back to the same minus input through resistor *Rf*.
- The plus input is connected to ground. Since the signal *V*1 is essentially applied to the minus input, the resulting output is opposite in phase to the input signal.

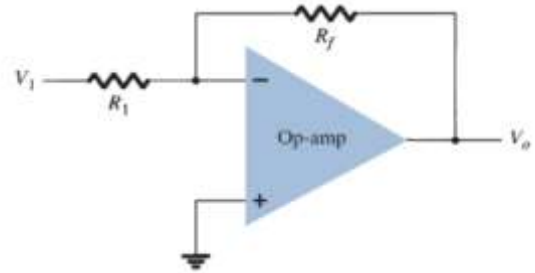
Figure shows the op-amp replaced by its ac equivalent circuit.

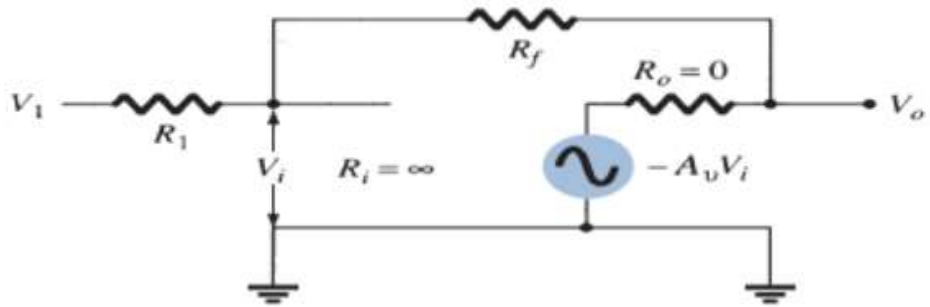


Basic op-amp connection.

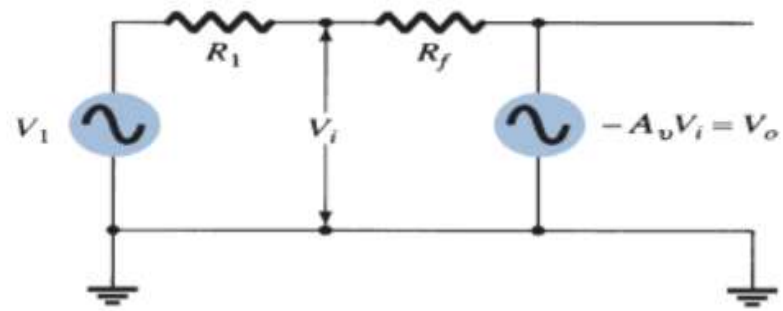


(a)





(b)

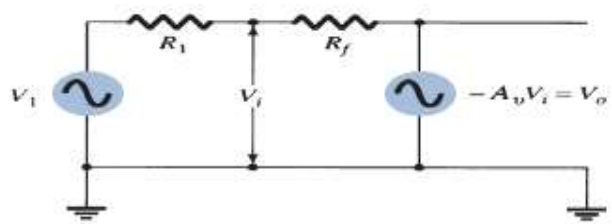


(c)

Operation of op-amp as constant-gain multiplier: (a) op-amp ac equivalent circuit; (b) ideal op-amp equivalent circuit; (c) redrawn equivalent circuit.

Using superposition, we can solve for the voltage V_1 in terms of the components due to each of the sources. For source V_1 only ($-A_v V_i$ set to zero),

$$V_{i_1} = \frac{R_f}{R_1 + R_f} V_1$$



For source $-A_v V_i$ only (V_1 set to zero),

$$V_{i_2} = \frac{R_1}{R_1 + R_f}(-A_v V_i)$$

The total voltage V_i is then

$$V_i = V_{i_1} + V_{i_2} = \frac{R_f}{R_1 + R_f} V_1 + \frac{R_1}{R_1 + R_f}(-A_v V_i)$$

which can be solved for V_i as

$$V_i = \frac{R_f}{R_f + (1 + A_v)R_1} V_1$$

If $A_v \gg 1$ and $A_v R_1 \gg R_f$, as is usually true, then

$$V_i = \frac{R_f}{A_v R_1} V_1$$

Solving for V_o/V_i, we get

$$\frac{V_o}{V_i} = \frac{-A_v V_i}{V_i} = \frac{-A_v}{V_i} \frac{R_f V_1}{A_v R_1} = -\frac{R_f}{R_1} \frac{V_1}{V_i}$$

so that

$$\boxed{\frac{V_o}{V_1} = -\frac{R_f}{R_1}}$$

The result in Eq. shows that the ratio of overall output to input voltage is dependent only on the values of resistors R_1 and R_f—provided that A_v is very large.

Unity Gain

If $R_f = R_1$, the gain is

$$\text{Voltage gain} = -\frac{R_f}{R_1} = -1$$

so that the circuit provides a unity voltage gain with 180° phase inversion. If R_f is exactly R_1, the voltage gain is exactly 1.

Constant-Magnitude Gain

If R_f is some multiple of R_1, the overall amplifier gain is a constant. For example, if $R_f = 10R_1$, then

$$\text{Voltage gain} = -\frac{R_f}{R_1} = -10$$

and the circuit provides a voltage gain of exactly 10 along with a 180° phase inversion from the input signal. If we select precise resistor values for R_f and R_1, we can obtain a wide range of gains, the gain being as accurate as the resistors used and is only slightly affected by temperature and other circuit factors.

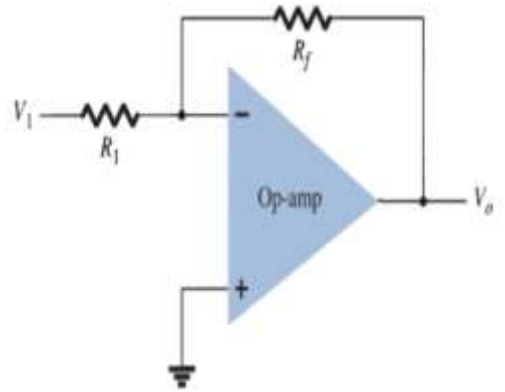
Virtual Ground:

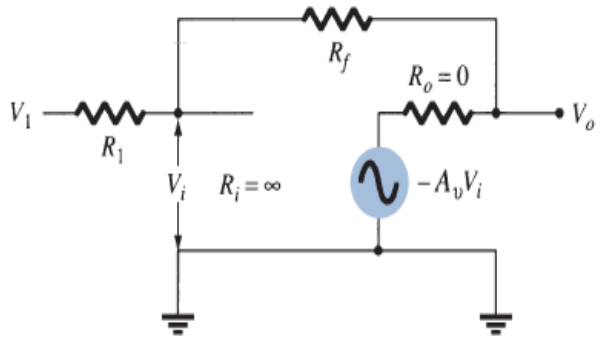
The output voltage is limited by the supply voltage of, typically, a few volts. As stated before, voltage gains are very high. If, for example, $V_o = -10$ V and $A_v = 20{,}000$, the input voltage is

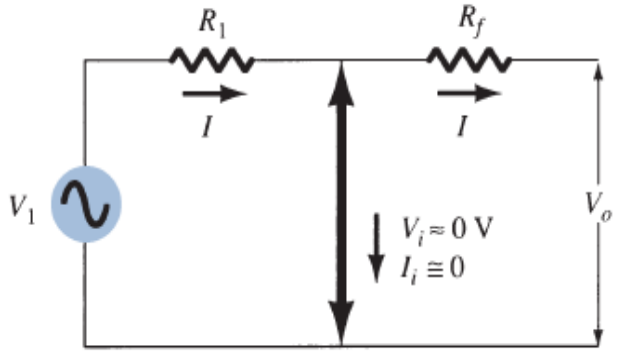
$$V_i = \frac{-V_o}{A_v} = \frac{10\text{ V}}{20{,}000} = 0.5\text{ mV}$$

If the circuit has an overall gain (V_o/V_1) of, say, 1, the value of V_1 is 10 V. Compared to all other input and output voltages, the value of V_i is then small and may be considered 0 V.

Note that although $V_i \approx 0$ V, it is not exactly 0 V. (The output voltage is a few volts due to the very small input V_i times a very large gain A_v.) The fact that $V_i \approx 0$ V leads to the concept that at the amplifier input there exists a virtual short-circuit or virtual ground.







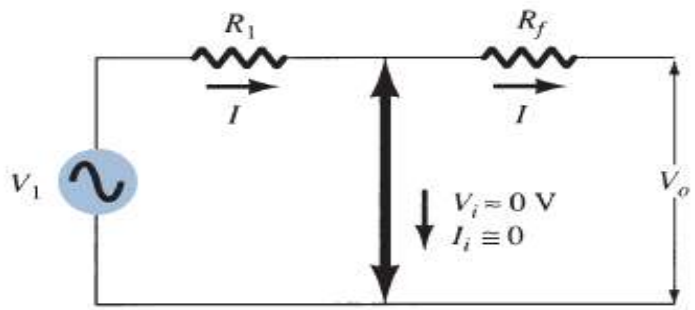
The concept of a virtual short implies that although the voltage is nearly 0 V, there is no current through the amplifier input to ground. Figure depicts the virtual ground concept. The heavy line is used to indicate that we may consider that a short exists with $V_i \approx 0$ V but that this is a virtual short so that no current goes through the short to ground. Current goes only through resistors R_1 and R_f as shown.

Using the virtual ground concept, we can write equations for the current I as follows:

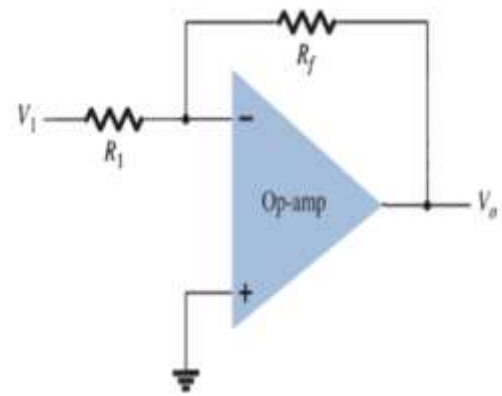
$$I = \frac{V_1}{R_1} = -\frac{V_o}{R_f}$$

which can be solved for V_o/V_1:

$$\frac{V_o}{V_1} = -\frac{R_f}{R_1}$$

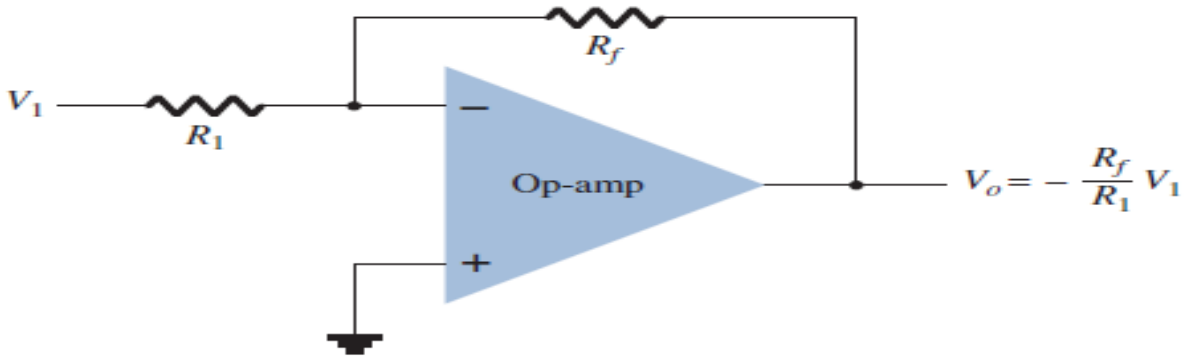


Virtual ground in an op-amp.



Inverting Amplifier:

$$V_o = -\frac{R_f}{R_1} V_1$$

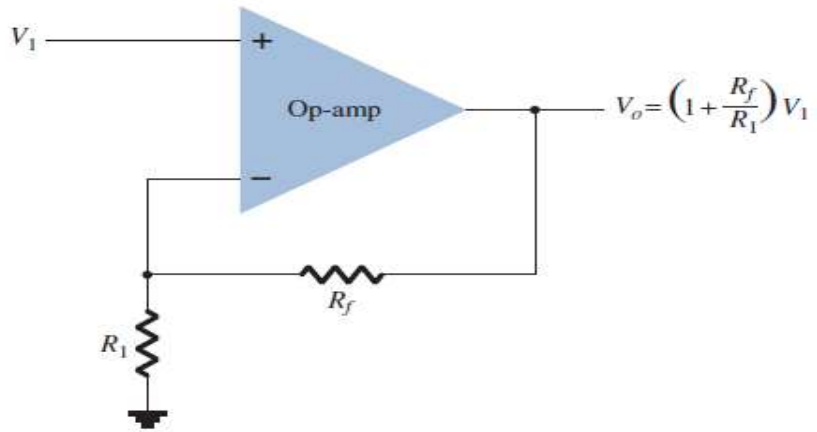


EXAMPLE 5 If the circuit of Fig. 34 has $R_1 = 100\,\text{k}\Omega$ and $R_f = 500\,\text{k}\Omega$, what output voltage results for an input of $V_1 = 2\,\text{V}$?

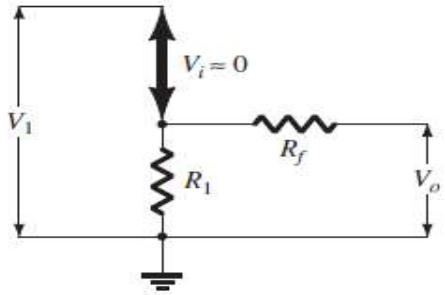
Solution:

$$\text{Eq. (8):} \quad V_o = -\frac{R_f}{R_1} V_1 = -\frac{500\,\text{k}\Omega}{100\,\text{k}\Omega}(2\,\text{V}) = \mathbf{-10\,V}$$

Noninverting Amplifier:



(a)



(b)

Non-inverting constant-gain multiplier.

$$V_1 = \frac{R_1}{R_1 + R_f} V_o$$

which results in

$$\frac{V_o}{V_1} = \frac{R_1 + R_f}{R_1} = 1 + \frac{R_f}{R_1}$$

EXAMPLE Calculate the output voltage of a noninverting amplifier (as in Fig.) for values of $V_1 = 2\,\text{V}$, $R_f = 500\,\text{k}\Omega$, and $R_1 = 100\,\text{k}\Omega$.

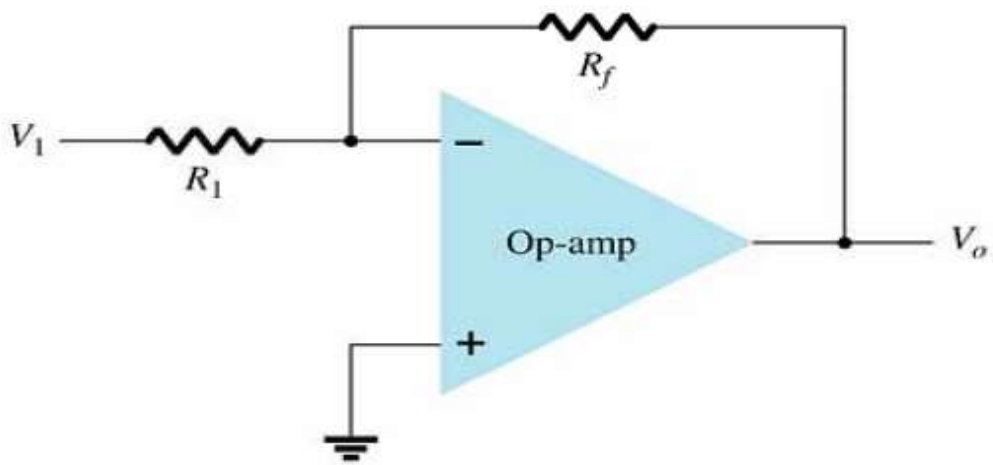
Solution:

$$\therefore \quad V_o = \left(1 + \frac{R_f}{R_1}\right) V_1 = \left(1 + \frac{500\,\text{k}\Omega}{100\,\text{k}\Omega}\right)(2\,\text{V}) = 6(2\,\text{V}) = \mathbf{+12\,V}$$

Inverting/Noninverting Op-Amps

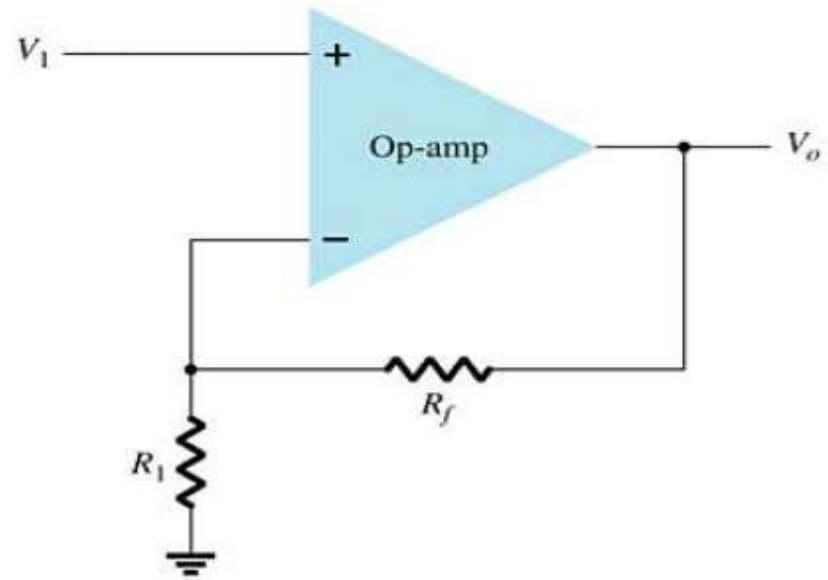
Inverting Amplifier

$$V_o = \frac{-R_f}{R_1} V_1$$



Noninverting Amplifier

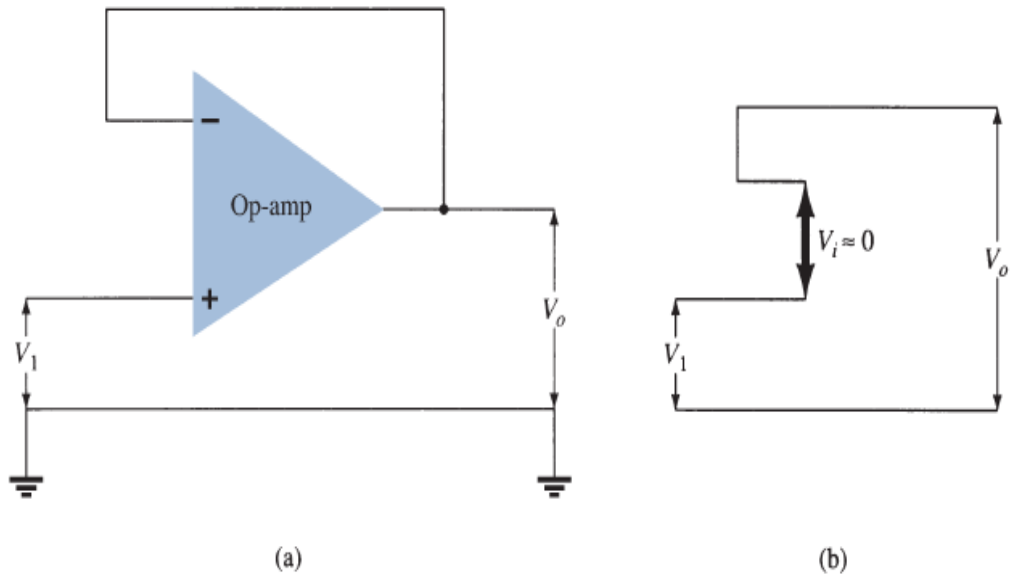
$$V_o = (1 + \frac{R_f}{R_1}) V_1$$



Unity follower:

The unity-follower circuit, as shown in Fig. provides a gain of unity (1) with no polarity or phase reversal. From the equivalent circuit it is clear that

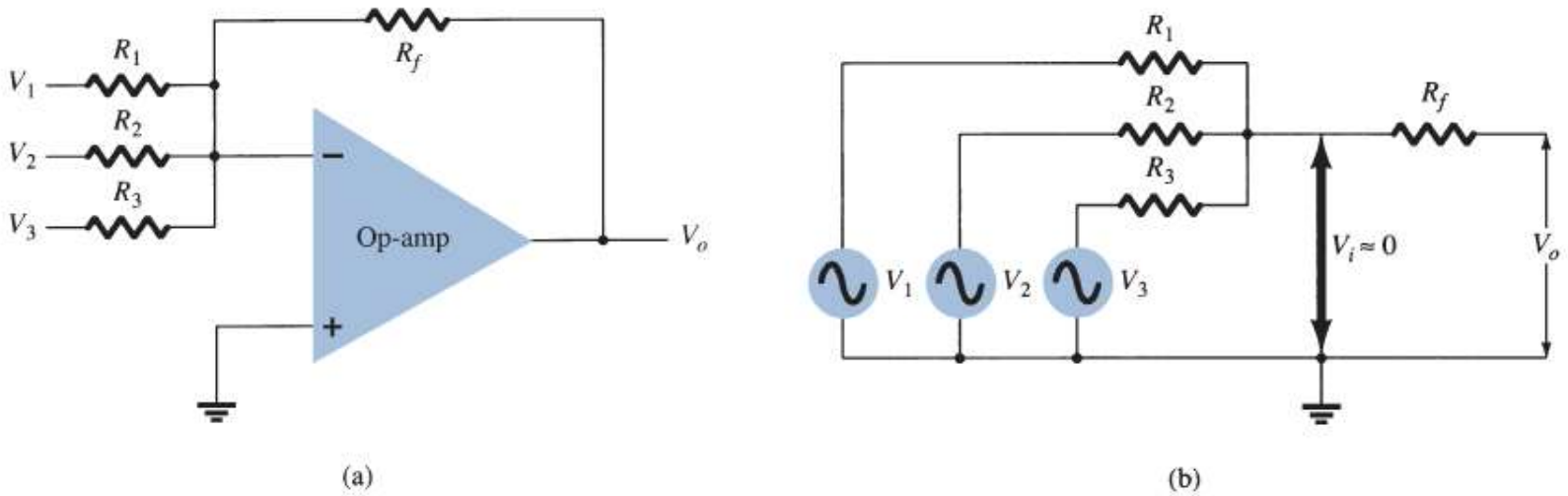
$$V_o = V_1$$



(a) Unity follower; (b) virtual-ground equivalent circuit.

Summing Amplifier:

$$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$$



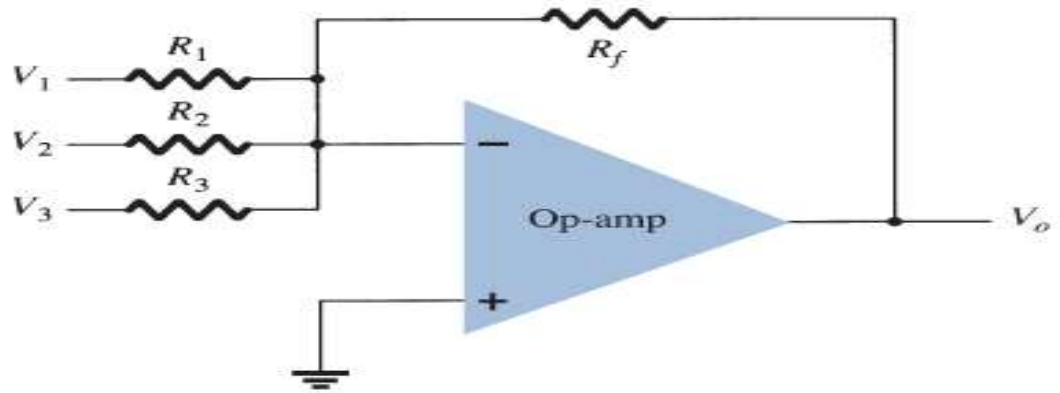
(a) Summing amplifier; (b) virtual-ground equivalent circuit.

The circuit shows a three-input summing amplifier circuit, which provides a means of algebraically summing (adding) three voltages, each multiplied by a constant-gain

factor. Using the equivalent representation shown in Fig., we can express the output voltage in terms of the inputs as

$$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$$

In other words, each input adds a voltage to the output multiplied by its separate constant-gain multiplier. If more inputs are used, they each add an additional component to the output.



EXAMPLE 7 Calculate the output voltage of an op-amp summing amplifier for the following sets of voltages and resistors. Use $R_f = 1\ \text{M}\Omega$ in all cases.

a. $V_1 = +1\ \text{V}, V_2 = +2\ \text{V}, V_3 = +3\ \text{V}, R_1 = 500\ \text{k}\Omega, R_2 = 1\ \text{M}\Omega, R_3 = 1\ \text{M}\Omega.$
b. $V_1 = -2\ \text{V}, V_2 = +3\ \text{V}, V_3 = +1\ \text{V}, R_1 = 200\ \text{k}\Omega, R_2 = 500\ \text{k}\Omega, R_3 = 1\ \text{M}\Omega.$

Solution: Using Eq. (11), we obtain

a. $$V_o = -\left[\frac{1000\ \text{k}\Omega}{500\ \text{k}\Omega}(+1\ \text{V}) + \frac{1000\ \text{k}\Omega}{1000\ \text{k}\Omega}(+2\ \text{V}) + \frac{1000\ \text{k}\Omega}{1000\ \text{k}\Omega}(+3\ \text{V})\right]$$
$$= -[2(1\ \text{V}) + 1(2\ \text{V}) + 1(3\ \text{V})] = \mathbf{-7\ V}$$

b. $$V_o = -\left[\frac{1000\ \text{k}\Omega}{200\ \text{k}\Omega}(-2\ \text{V}) + \frac{1000\ \text{k}\Omega}{500\ \text{k}\Omega}(+3\ \text{V}) + \frac{1000\ \text{k}\Omega}{1000\ \text{k}\Omega}(+1\ \text{V})\right]$$
$$= -[5(-2\ \text{V}) + 2(3\ \text{V}) + 1(1\ \text{V})] = \mathbf{+3\ V}$$

Contents of the Class:

- Integrator
- Differentiator
- Off-set error voltages and currents
- Frequency Parameters
- measurement of OPAMP parameters and its frequency response
- Active filters

- Referred Book:- R L Boylestad

Integrator:

If the feedback component used is a capacitor, as shown in Fig. the resulting connection is called an *integrator.*

The virtual-ground equivalent circuit shows that an expression for the voltage between input and output can be derived in terms of the current *I* from input to output.

$$X_C = \frac{1}{j\omega C} = \frac{1}{sC}$$

where $s = j\omega$ is in the Laplace notation.* Solving for V_o/V_1 yields

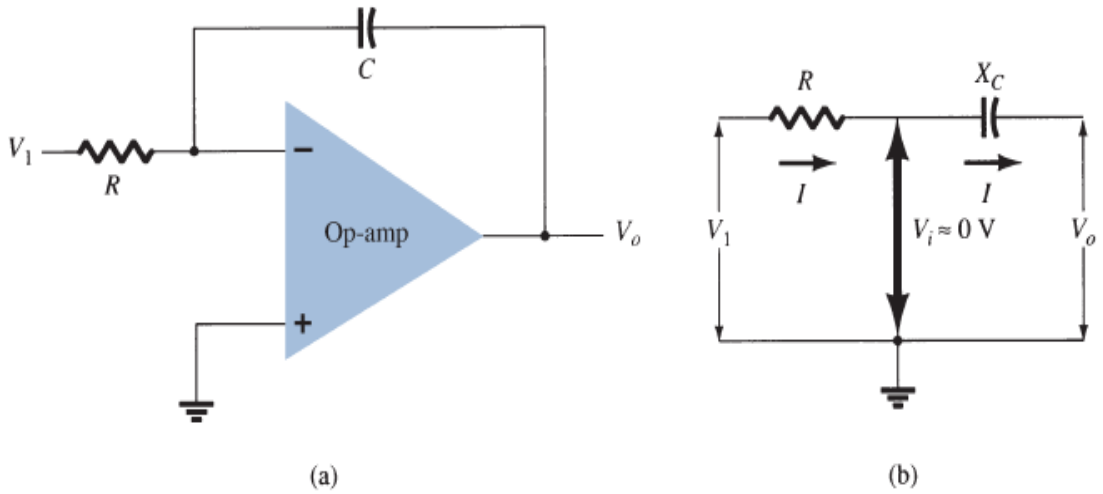
$$I = \frac{V_1}{R} = -\frac{V_o}{X_C} = \frac{-V_o}{1/sC} = -sCV_o$$

$$\frac{V_o}{V_1} = \frac{-1}{sCR}$$

This expression can be rewritten in the time domain as

$$v_o(t) = -\frac{1}{RC}\int v_1(t)\,dt$$

Equation shows that the output is the integral of the input, with an inversion and scale multiplier of 1/*RC*. The ability to integrate a given signal provides the analog computer with the ability to solve differential equations and therefore provides the ability to electrically solve analogs of physical system operation.

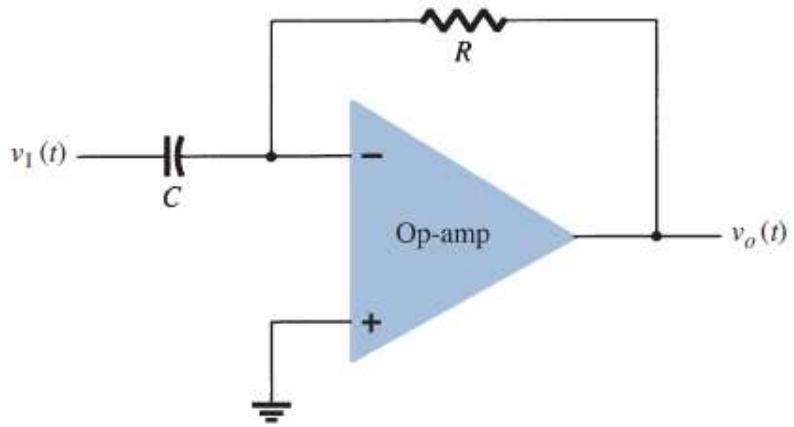


Integrator.

Differentiator:

$$v_o(t) = -RC\frac{dv_1(t)}{dt}$$

where the scale factor is -*RC*.



Differentiator circuit.

OP-AMP SPECIFICATIONS—DC Offset Parameters:

Offset Currents and voltages

Although the op-amp output should be 0 V when the input is 0 V, in actual operation there is some offset voltage at the output. For example, if one connected 0 V to both op-amp inputs and then measured 26 mV(dc) at the output, this would represent 26 mV of unwanted voltage generated by the circuit and not by the input signal.

Since the user may connect the
amplifier circuit for various gain and polarity operations, however, the manufacturer specifies
an input offset voltage for the op-amp.

The output offset voltage can be shown to be affected by two separate circuit conditions: (1) an input offset voltage V_{IO} and (2) an offset current due to the difference in currents resulting at the plus (+) and minus (−) inputs.

$$V_o = AV_i = A\left(V_{IO} - V_o\frac{R_1}{R_1 + R_f}\right)$$

Input Offset voltage V_{IO}

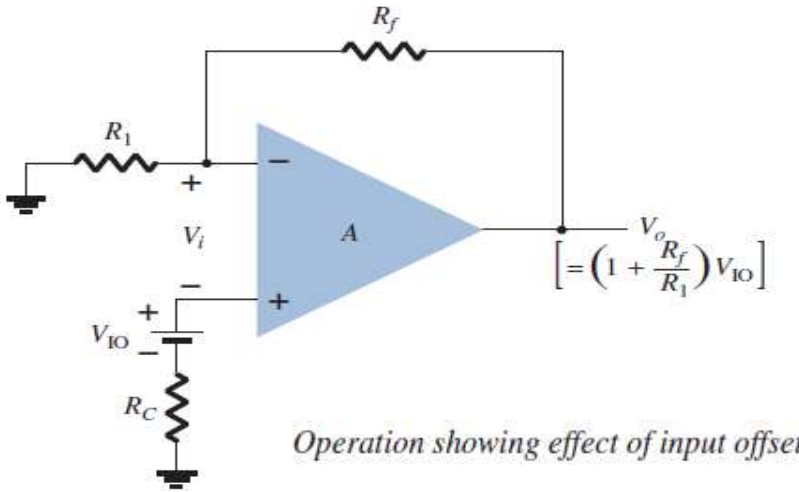
The manufacturer's specification sheet provides a value of V_{IO} for the op-amp.

Solving for V_o, we get

$$V_o = V_{IO}\frac{A}{1 + A\left[R_1/(R_1 + R_f)\right]} \approx V_{IO}\frac{A}{A\left[R_1/(R_1 + R_f)\right]}$$

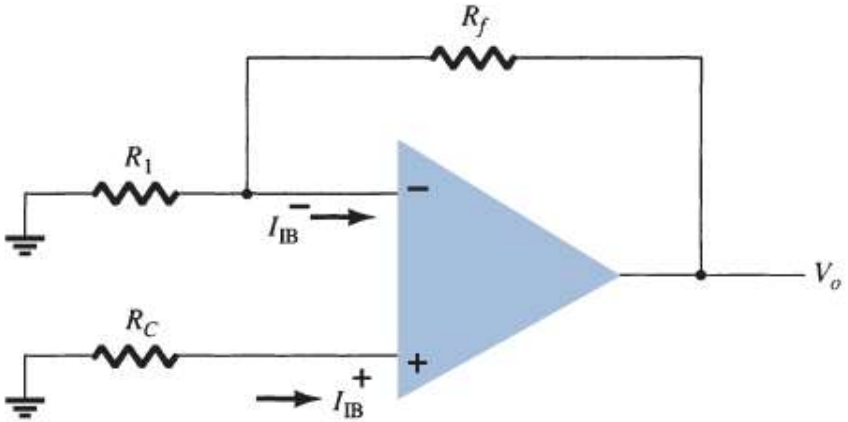
from which we can write

$$V_o(\text{offset}) = V_{IO}\frac{R_1 + R_f}{R_1}$$

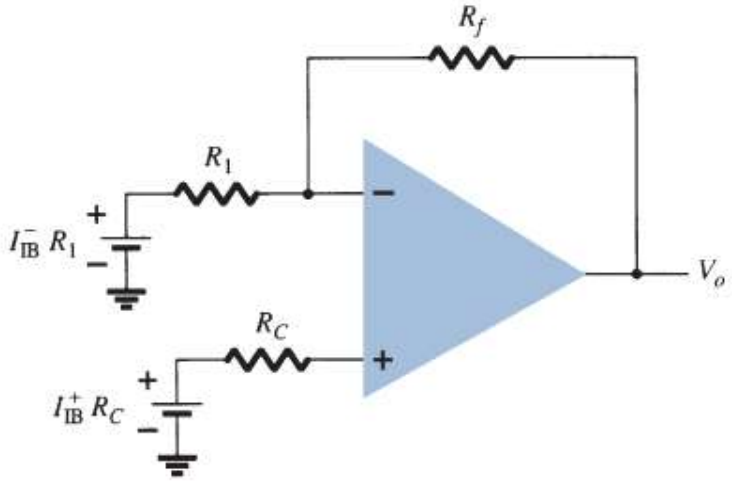


Operation showing effect of input offset voltage V_{IO}.

Output Offset voltage due to input Offset Current I_{IO}



Op-amp connection showing input bias currents.



Redrawn circuit

An output offset voltage will also result due to any difference in dc bias currents at both inputs. Since the two input transistors are never exactly matched, each will operate at a slightly different current.

Replacing the bias currents through the input resistors by the voltage drop that each develops as shown in Fig.

the resulting output voltage. Using superposition, we see that the output voltage due to input bias current I_{IB}^{+}, denoted by V_o^{+}, is given by

$$V_o^{+} = I_{\text{IB}}^{+} R_C \left(1 + \frac{R_f}{R_1}\right)$$

whereas the output voltage due to only I_{IB}^{-}, denoted by V_o^{-}, is given by

$$V_o^{-} = I_{\text{IB}}^{-} R_1 \left(-\frac{R_f}{R_1}\right)$$

for a total output offset voltage of

$$V_o(\text{offset due to } I_{\text{IB}}^{+} \text{ and } I_{\text{IB}}^{-}) = I_{\text{IB}}^{+} R_C \left(1 + \frac{R_f}{R_1}\right) - I_{\text{IB}}^{-} R_1 \frac{R_f}{R_1}$$

Since the main consideration is the difference between the input bias currents rather than each value, we define the offset current I_{IO} by

$$I_{\text{IO}} = I_{\text{IB}}^{+} - I_{\text{IB}}^{-}$$

Since the compensating resistance R_C is usually approximately equal to the value of R_1, using $R_C = R_1$ in Eq. (17), we can write

$$\begin{aligned} V_o(\text{offset}) &= I_{\text{IB}}^{+}(R_1 + R_f) - I_{\text{IB}}^{-} R_f \\ &= I_{\text{IB}}^{+} R_f - I_{\text{IB}}^{-} R_f = R_f(I_{\text{IB}}^{+} - I_{\text{IB}}^{-}) \end{aligned}$$

resulting in

$$\boxed{V_o\,(\text{offset due to } I_{\text{IO}}) = I_{\text{IO}} R_f}$$

Total Offset Due to V_{IO} and I_{IO} Since the op-amp output may have an output offset voltage due to both factors covered above, the total output offset voltage can be expressed as

$$|V_o(\text{offset})| = |V_o(\text{offset due to} V_{IO})| + |V_o(\text{offset due to } I_{IO})|$$

The absolute magnitude is used to accommodate the fact that the offset polarity may be either positive or negative.

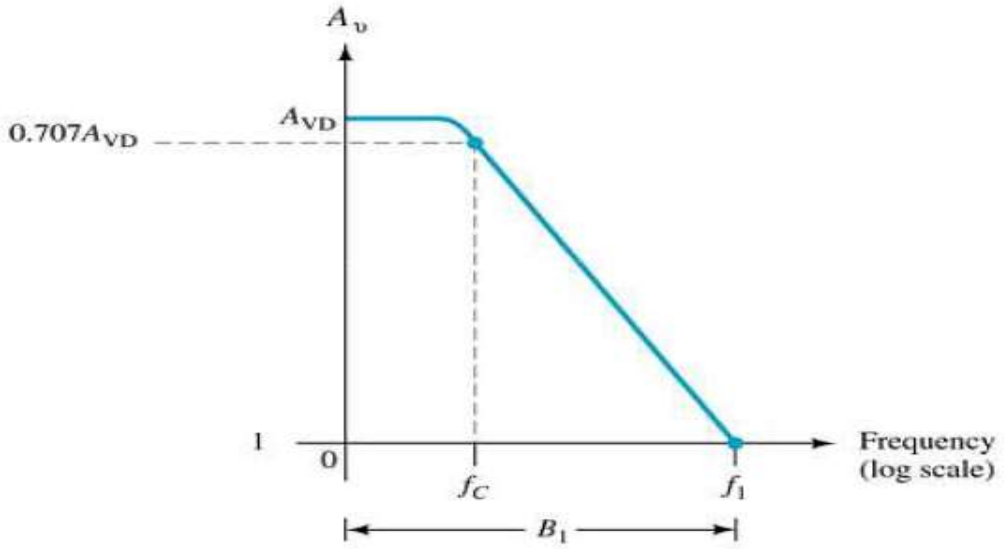
Frequency Parameters:

An op-amp is a wide-bandwidth amplifier. The following affect the bandwidth of the op-amp:

- Gain
- Slew rate

Gain and Bandwidth

The op-amp's high frequency response is limited by internal circuitry. The plot shown is for an open loop gain (A_{OL} or A_{VD}). This means that the op-amp is operating at the highest possible gain with no feedback resistor. In the open loop, the op-amp has a narrow bandwidth. The bandwidth widens in closed loop operation, but then the gain is lower.



the unity-gain frequency and cutoff frequency are related by

$$f_1 = A_{VD} f_C$$

Equation shows that the unity-gain frequency may also be called the gain–bandwidth product of the op-amp.

Slew Rate (SR):

Slew rate = maximum rate at which amplifier output can change in volts per microsecond ($V/\mu s$)

$$SR = \frac{\Delta V_o}{\Delta t} \text{ V}/\mu\text{s} \quad \text{with } t \text{ in } \mu\text{s}$$

The slew rate provides a parameter specifying the maximum rate of change of the output voltage when driven by a large step-input signal.* If one tried to drive the output at a rate

of voltage change greater than the slew rate, the output would not be able to change fast enough and would not vary over the full range expected, resulting in signal clipping or distortion. In any case, the output would not be an amplified duplicate of the input signal if the op-amp slew rate were to be exceeded.

Maximum Signal Frequency

The maximum frequency at which an op-amp may operate depends on both the bandwidth (BW) and slew rate (SR) parameters of the op-amp. For a sinusoidal signal of general form

$$v_o = K \sin(2\pi ft)$$

the maximum voltage rate of change can be shown to be

$$\text{signal maximum rate of change} = 2\pi fK \text{ V/s}$$

To prevent distortion at the output, the rate of change must also be less than the slew rate, that is,

$$2\pi fK \leq \text{SR}$$
$$\omega K \leq \text{SR}$$

so that

$$f \leq \frac{\text{SR}}{2\pi K} \quad \text{Hz}$$
$$\omega \leq \frac{\text{SR}}{K} \quad \text{rad/s}$$

General Op-Amp Specifications

Other ratings for op-amp found on specification sheets are:

- **Absolute Ratings**
- **Electrical Characteristics**
- **Performance**

Absolute Ratings

These are common maximum ratings for the op-amp.

Absolute Maximum Ratings	
Supply voltage	6 22 V
Internal power dissipation	500 mW
Differential input voltage	6 30 V
Input voltage	6 15 V

Electrical Characteristics

TABLE 13.2 mA741 Electrical Characteristics: $V_{CC} = \pm 15$ V, $T_A = 25°C$

Characteristic	*MIN*	*TYP*	*MAX*	*Unit*
V_{IO} Input offset voltage		1	6	mV
I_{IO} Input offset current		20	200	nA
I_{IB} Input bias current		80	500	nA
V_{ICR} Common-mode input voltage range	±12	±13		V
V_{OM} Maximum peak output voltage swing	±12	±14		V
A_{VD} Large-signal differential voltage amplification	20	200		V/mV
r_i Input resistance	0.3	2		MΩ
r_o Output resistance		75		Ω
C_i Input capacitance		1.4		pF
CMRR Common-mode rejection ratio	70	90		dB
I_{CC} Supply current		1.7	2.8	mA
P_D Total power dissipation		50	85	mW

Note: These ratings are for specific circuit conditions, and they often include minimum, maximum and typical values.

CMRR

One rating that is unique to op-amps is CMRR or common-mode rejection ratio.

Because the op-amp has two inputs that are opposite in phase (inverting input and the non-inverting input) any signal that is common to both inputs will be cancelled.

Op-amp CMRR is a measure of the ability to cancel out common-mode signals.

Differential and Common-Mode Operation:

- op-amp, is the circuit's ability to greatly amplify signals that are opposite at the two inputs while only slightly amplifying signals that are common to both inputs.
- An op-amp provides an output component that is due to the amplification of the difference of the signals applied to the plus and minus inputs and a component due to the signals common to both inputs.
- Since amplification of the opposite input signals is much greater than that of the common input signals, the circuit provides a common-mode rejection as described by a numerical value called the common-mode rejection ratio (CMRR).

Differential Inputs

When separate inputs are applied to the op-amp, the resulting difference signal is the difference between the two inputs.

$$V_d = V_{i_1} - V_{i_2}$$

Common Inputs

When both input signals are the same, a common signal element due to the two inputs can be defined as the average of the sum of the two signals.

$$V_c = \tfrac{1}{2}(V_{i_1} + V_{i_2})$$

Output Voltage

Since any signals applied to an op-amp in general have both in-phase and out-of-phase components, the resulting output can be expressed as

$$V_o = A_d V_d + A_c V_c$$

where V_d = difference voltage
V_c = common voltage
A_d = differential gain of the amplifier
A_c = common-mode gain of the amplifier

Common-Mode Rejection Ratio

Having obtained A_d and A_c (as in the measurement procedure discussed above), we can now calculate a value for the common-mode rejection ratio (CMRR), which is defined by the following equation:

$$\text{CMRR} = \frac{A_d}{A_c}$$

The value of CMRR can also be expressed in logarithmic terms as

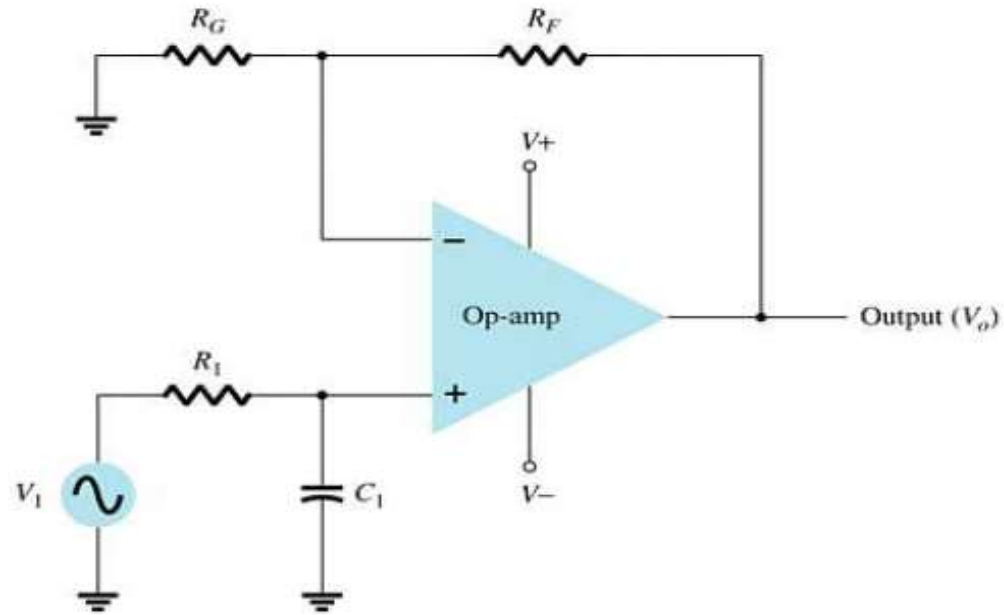
$$\text{CMRR (log)} = 20 \log_{10} \frac{A_d}{A_c} \quad \text{(dB)}$$

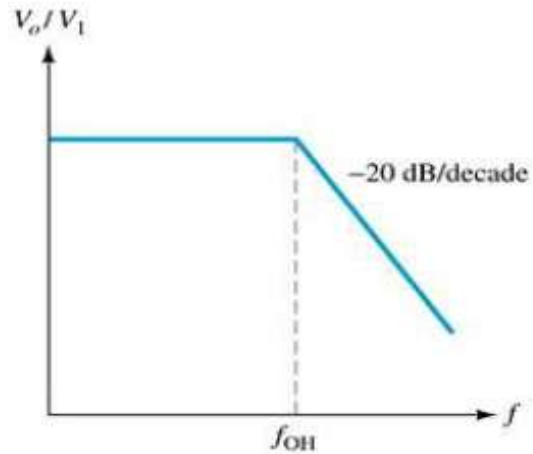
Active Filters

Adding capacitors to op-amp circuits provides external control of the cutoff frequencies. The op-amp active filter provides controllable cutoff frequencies and controllable gain.

- **Low-pass filter**
- **High-pass filter**
- **Bandpass filter**

Low-Pass Filter—First-Order

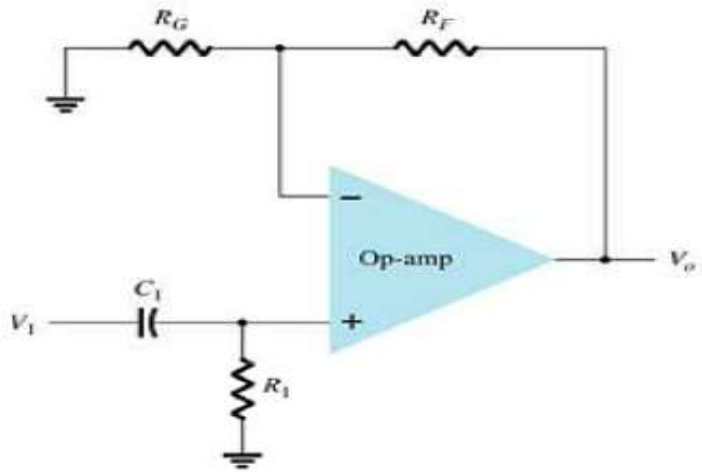


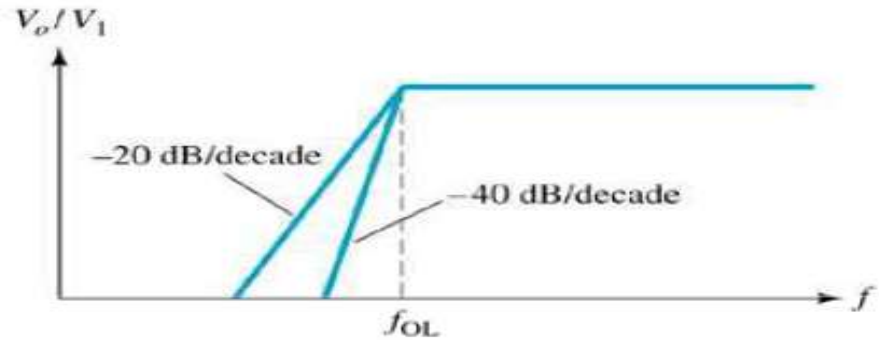


The upper cutoff frequency and voltage gain are given by:

$$f_{OH} = \frac{1}{2\pi R_1 C_1} \qquad A_v = 1 + \frac{R_f}{R_1}$$

High-Pass Filter



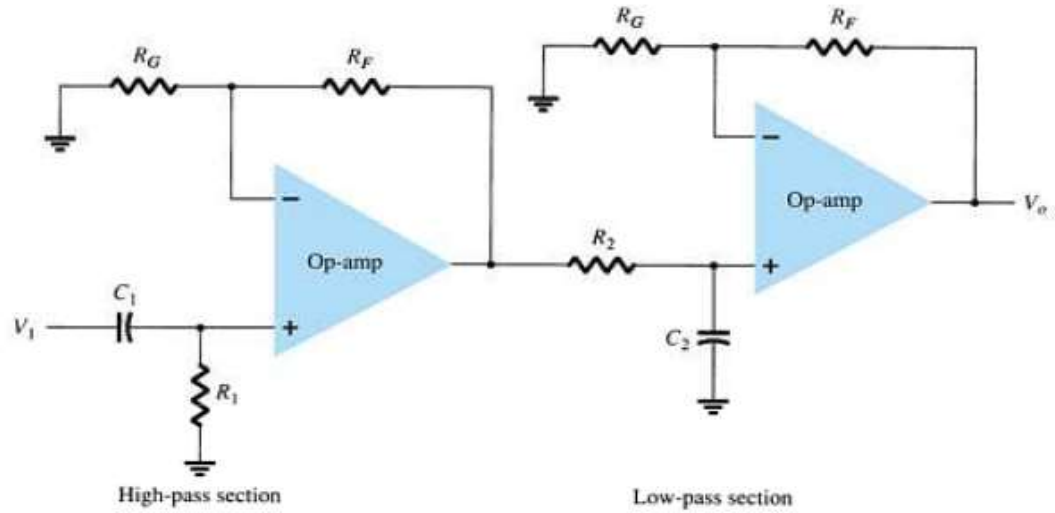


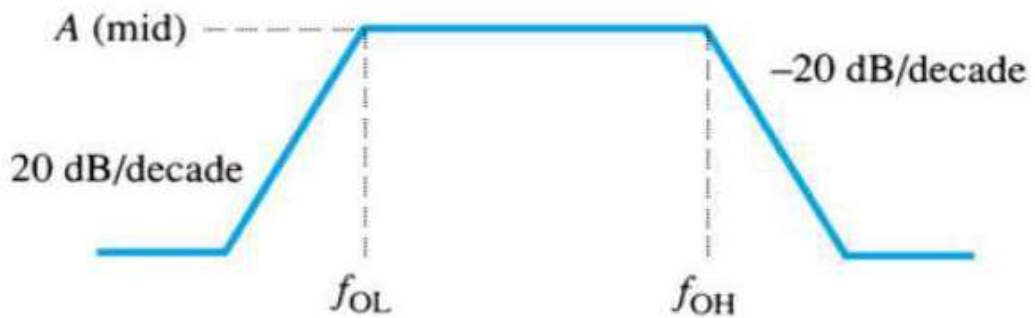
The cutoff frequency is determined by:

$$f_{OL} = \frac{1}{2\pi R_1 C_1}$$

Bandpass Filter

There are two cutoff frequencies: upper and lower. They can be calculated using the same low-pass cutoff and high-pass cutoff frequency formulas in the appropriate sections.





Contents of the Class:

- Class –A large signal amplifier
- Transformer coupled audio amplifier,
- Class-B push-pull amplifier.
- higher order harmonic generation,

- Referred Book:- R L Boylestad

Power Amplifiers:

Definitions

In small-signal amplifiers the main factors are:

- **Amplification**
- **Linearity**
- **Gain**

Since large-signal, or power, amplifiers handle relatively large voltage signals and current levels, the main factors are:

- **Efficiency**
- **Maximum power capability**
- **Impedance matching to the output device**

Amplifier Types

Class A

The amplifier conducts through the full 360° of the input. The Q-point is set near the middle of the load line.

Class B

The amplifier conducts through 180° of the input. The Q-point is set at the cutoff point.

Class AB

This is a compromise between the class A and B amplifiers. The amplifier conducts somewhere between 180° and 360° . The Q-point is located between the mid-point and cutoff.

Class C

The amplifier conducts less than 180 of the input. The Q-point is located below the cutoff level.

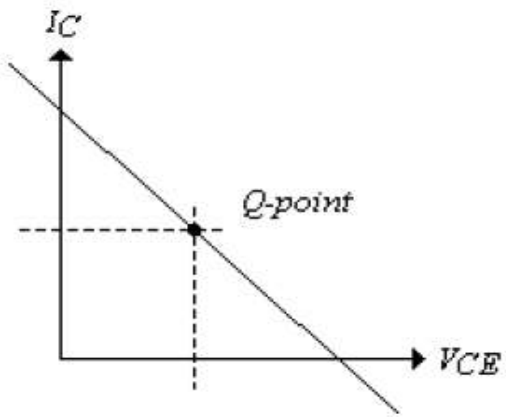
Class D

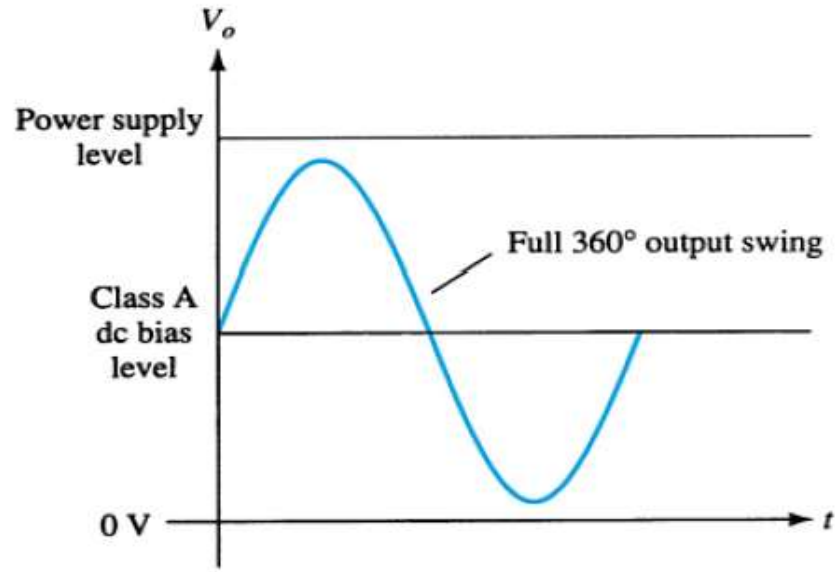
This is an amplifier that is biased especially for digital signals.

Class A Amplifier

The output of a class A amplifier conducts for the full 360° of the cycle.

The Q-point is set at the middle of the load line so that the AC signal can swing a full cycle.

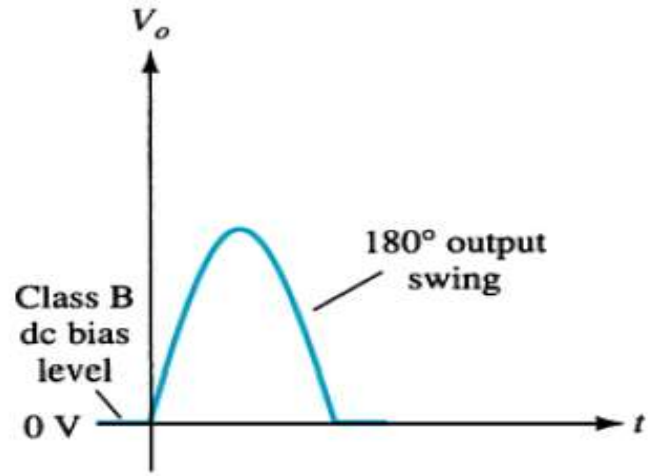


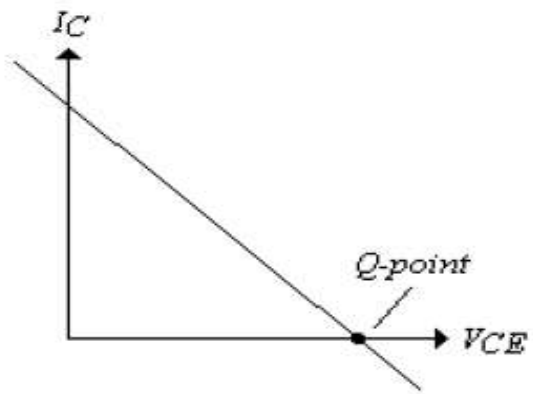


Remember that the DC load line indicates the maximum and minimum limits set by the DC power supply.

Class B Amplifier

A class B amplifier output only conducts for 180° or one-half of the AC input signal.



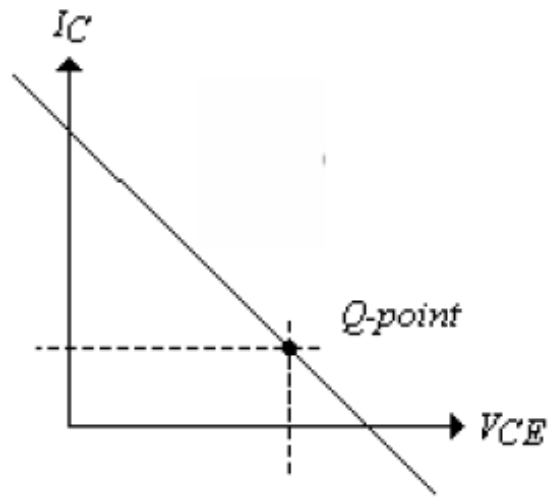


The Q-point is at 0V on the load line, so that the AC signal can only swing for one-half cycle.

Class AB Amplifier

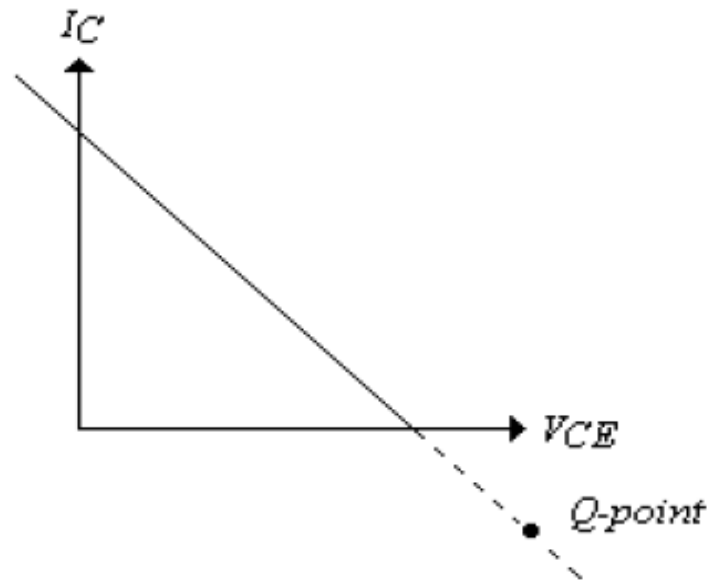
This amplifier is a compromise between the class A and class B amplifier—the Q-point is above that of the Class B but below the class A.

The output conducts between 180° and 360° of the AC input signal.



Class C

The output of the class C conducts for less than 180° of the AC cycle. The Q-point is below cutoff.



Amplifier Efficiency

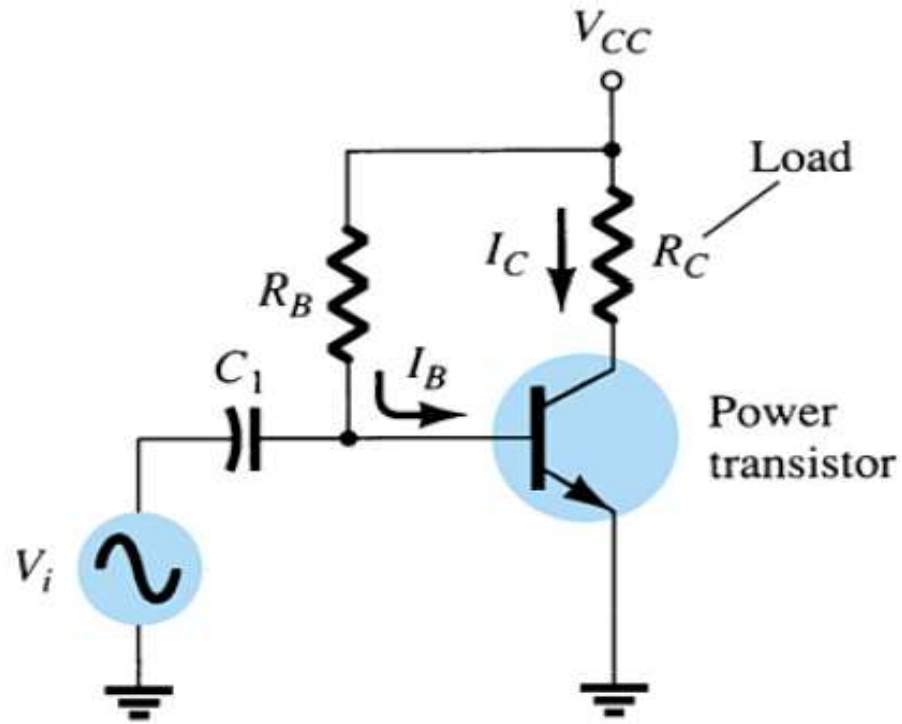
Comparison of Amplifier Classes					
	A	*AB*	*Class B*	*C**	*D*
Operating cycle	360°	180° to 360°	180°	Less than 180°	Pulse operation
Power efficiency	25% to 50%	Between 25% (50%) and 78.5%	78.5%		Typically over 90%

**Class C is usually not used for delivering large amounts of power, thus the efficiency is not given here.*

Efficiency refers to the ratio of output to input power. The lower the amount of conduction of the amplifier the higher the efficiency.

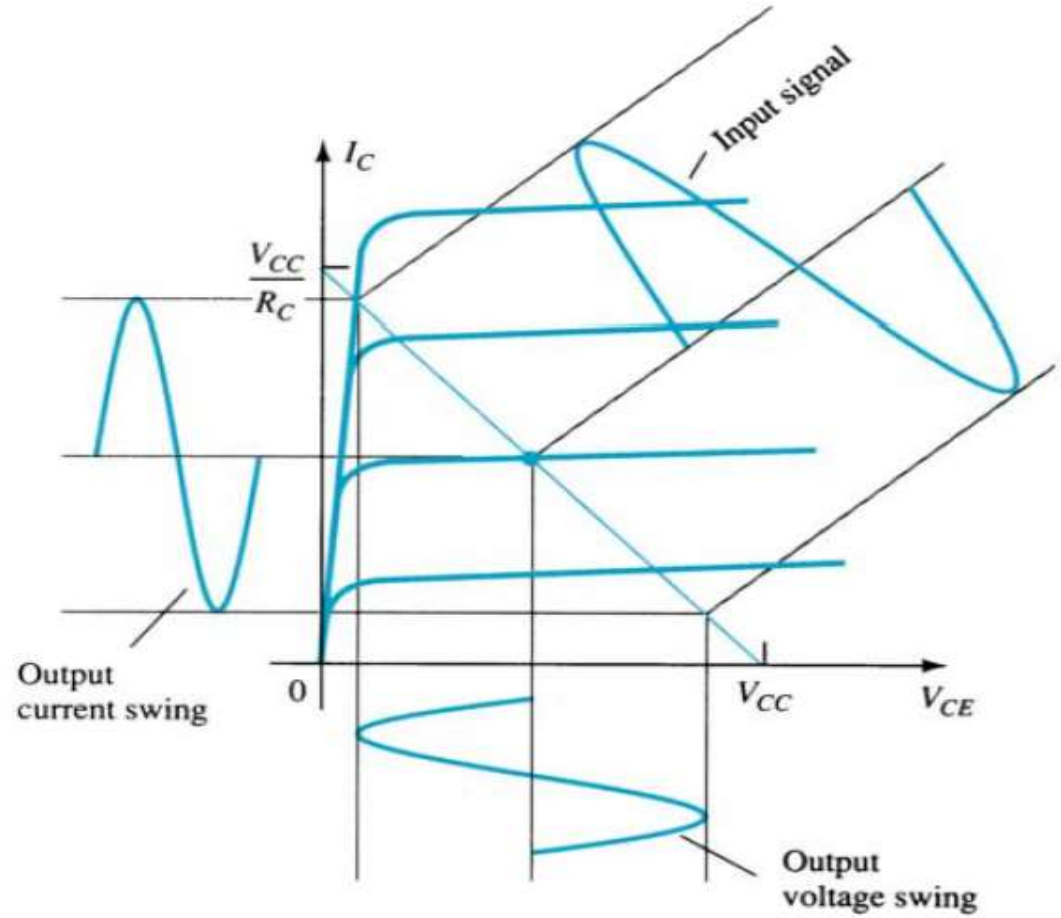
Series-Fed Class A Amplifier

This is similar to the small-signal amplifier except that it will handle higher voltages. The transistor used is a high-power transistor.



Series-Fed Class A Amplifier

A small input signal causes the output voltage to swing to a maximum of V_{cc} and a minimum of 0V. The current can also swing from 0mA to I_{CSAT} (V_{CC}/R_C)



Series-Fed Class A Amplifier

Input Power

The power into the amplifier is from the DC supply. With no input signal, the DC current drawn is the collector bias current, I_{CQ}.

$$P_{i(dc)} = V_{CC} I_{CQ}$$

Output Power

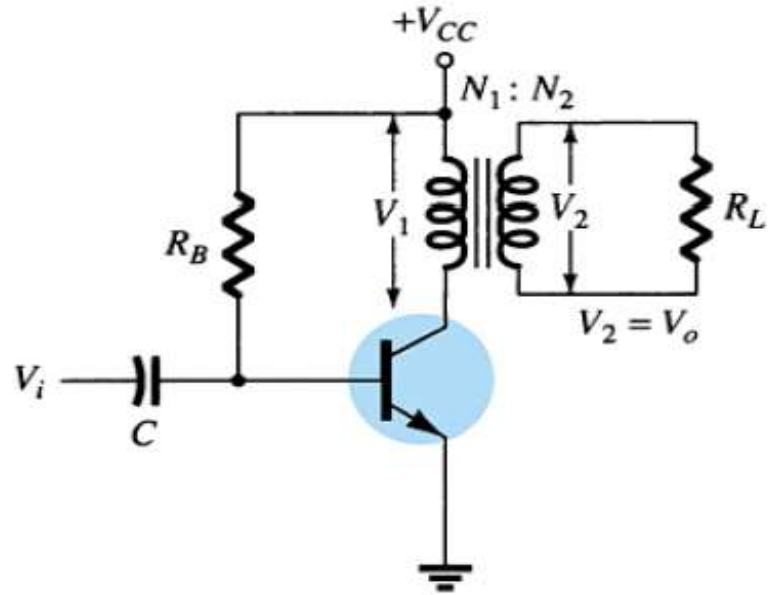
$$P_{o(ac)} = \frac{V^2_{C(rms)}}{R_C} \qquad \text{or} \qquad P_{o(ac)} = \frac{V^2_{CE(p-p)}}{8R_C}$$

Efficiency

$$\%\eta = \frac{P_{o(ac)}}{P_{i(ac)}} \times 100$$

Transformer-Coupled Class A Amplifier

This circuit uses a transformer to couple to the load. This improves the efficiency of the Class A to 50%.



Transformer Action

A transformer improves the efficiency because it is able to transform the voltage, current, and impedance

Voltage Ratio

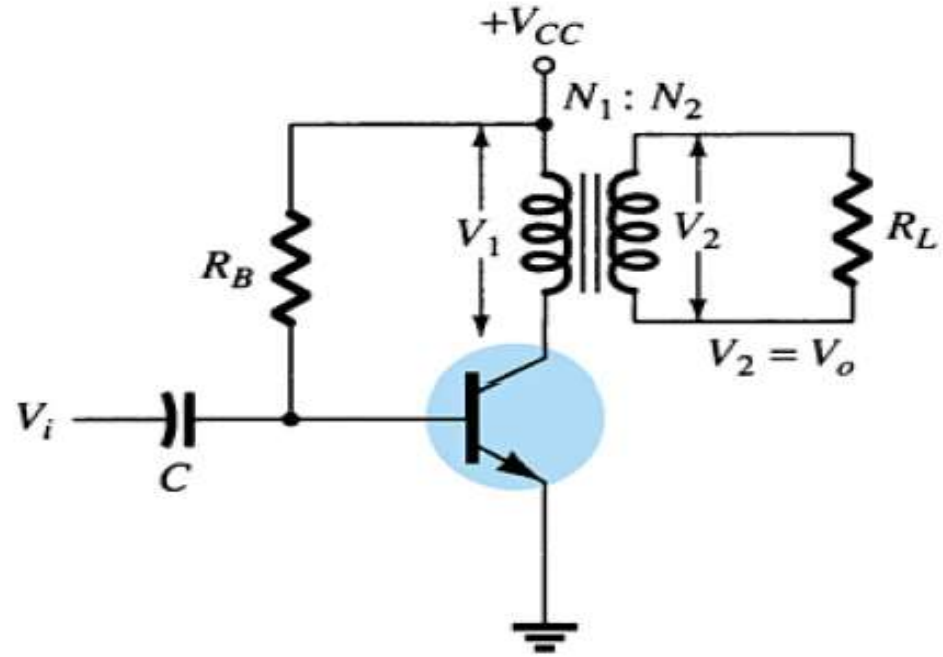
$$\frac{V_2}{V_1} = \frac{N_2}{N_1}$$

Current Ratio

$$\frac{I_2}{I_1} = \frac{N_1}{N_2}$$

Impedance Ratio

$$\frac{R'_L}{R_L} = \frac{R_1}{R_2} = \left(\frac{N_1}{N_2}\right)^2 = a^2$$



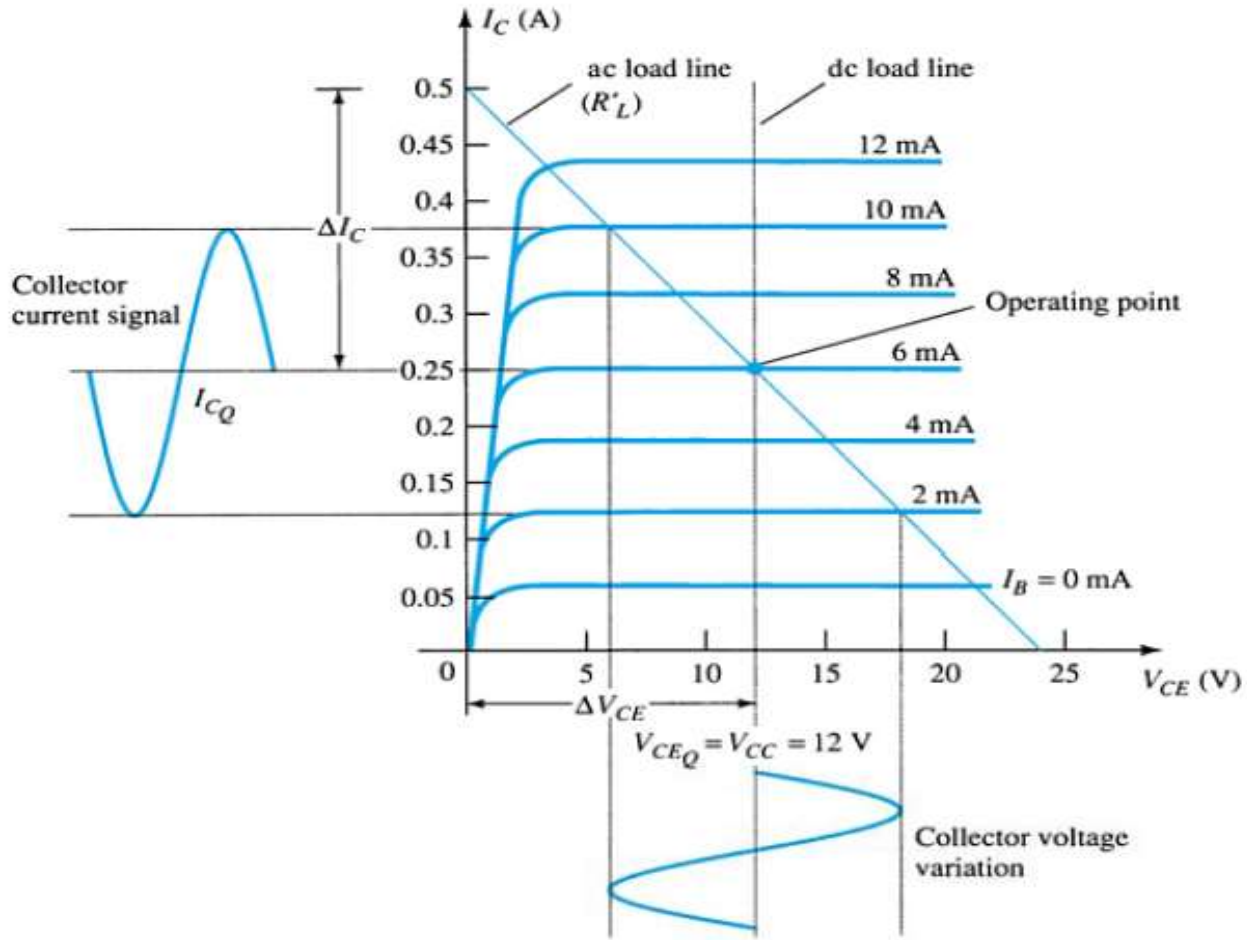
Transformer-Coupled Class A Amplifier

DC Load Line

As in all class A amplifiers the Q-point is established close to the midpoint of the DC load line.

AC Load Line

The saturation point (I_{Cmax}) is at V_{cc}/R'_L and the cutoff point is at V_2 (the secondary voltage of the transformer). This increases the maximum output swing because the minimum and maximum values of I_C and V_{CE} are spread further apart.



Transformer-Coupled Class A Amplifier

Signal Swing and Output AC Power

The voltage swing:

$$V_{CE(p-p)} = V_{CE\,max} - V_{CE\,min}$$

The current swing:

$$I_{C\,max} - I_{C\,min}$$

The AC power:

$$P_{o(ac)} = \frac{(V_{CEmax} - V_{CEmin})(I_{Cmax} - I_{Cmin})}{8}$$

Transformer-Coupled Class A Amplifier Efficiency

Power input from the DC source:

$$P_{i(dc)} = V_{CC} I_{CQ}$$

Power dissipated as heat across the transistor:

$$P_Q = P_{i(dc)} - P_{o(ac)}$$

Note: The larger the input and output signal, the lower the heat dissipation.

Maximum efficiency:

$$\%\eta = 50\left(\frac{V_{CEmax} - V_{CEmin}}{V_{CEmax} + V_{CEmin}}\right)^2$$

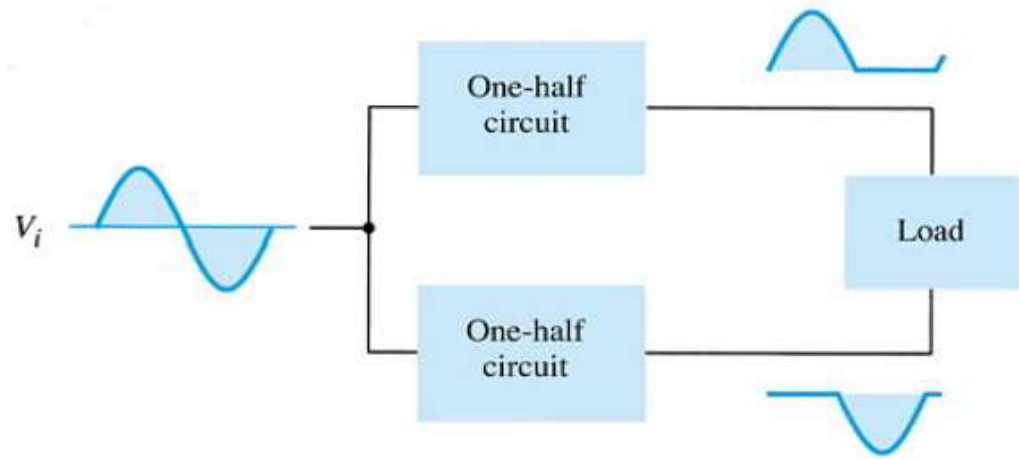
Note: The larger V_{CEmax} and smaller V_{CEmin}, the closer the efficiency approaches the theoretical maximum of 50%.

Class B Amplifier

In class B, the transistor is biased just off. The AC signal turns the transistor on.

The transistor only conducts when it is turned on by one-half of the AC cycle.

In order to get a full AC cycle out of a class B amplifier, you need two transistors:



- **An *npn* transistor that provides the negative half of the AC cycle**
- **A *pnp* transistor that provides the positive half.**

Class B Amplifier: Efficiency

The maximum efficiency of a class B is 78.5%..

$$\%\eta = \frac{P_{o(ac)}}{P_{i(dc)}} \times 100$$

$$\text{maximum } P_{o(dc)} = \frac{V_{CC}^2}{2R_L}$$

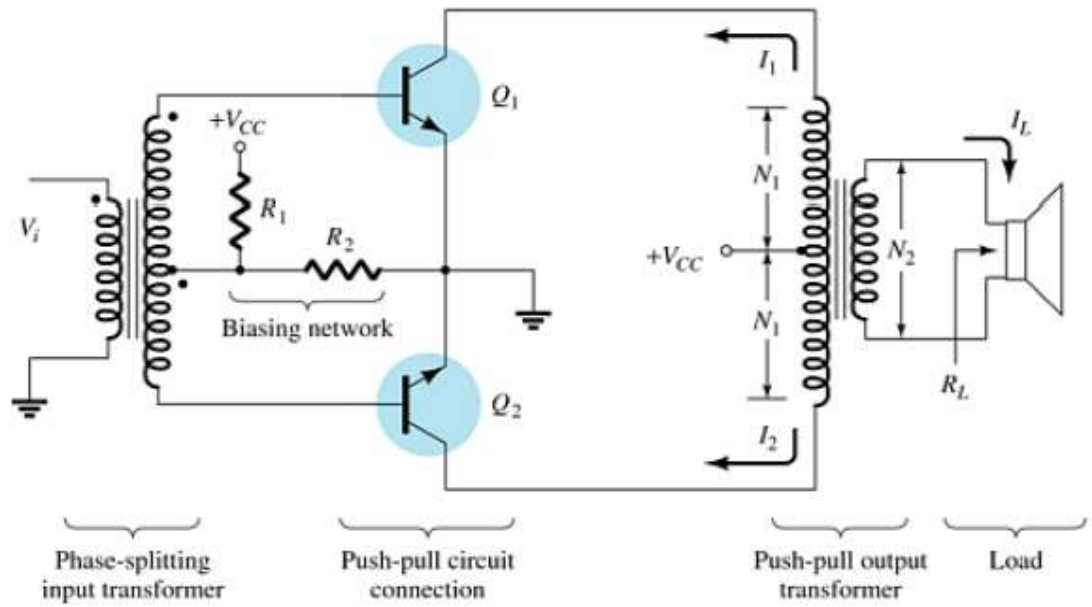
For maximum power, $V_L = V_{CC}$

$$\text{maximum } P_{i(dc)} = V_{CC}(\text{maximum } I_{dc}) = V_{CC}\left(\frac{2V_{CC}}{\pi R_L}\right) = \frac{2V^2{}_{CC}}{\pi R_L}$$

Transformer-Coupled Push-Pull Class B Amplifier

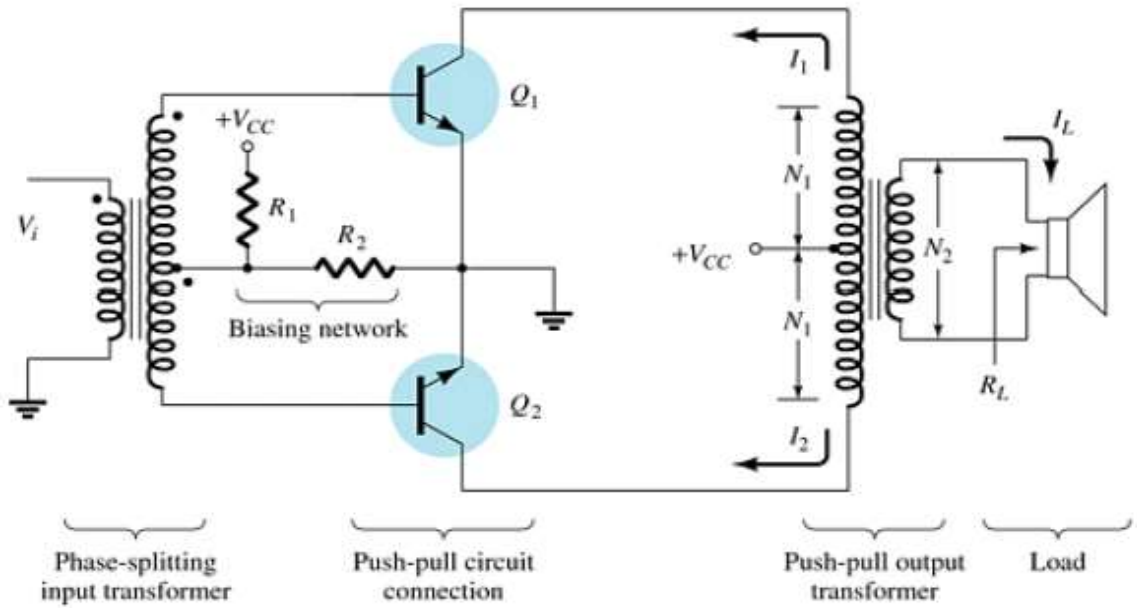
The center-tapped transformer on the input produces opposite polarity signals to the two transistor inputs.

The center-tapped transformer on the output combines the two halves of the AC waveform together.



Class B Amplifier Push-Pull Operation

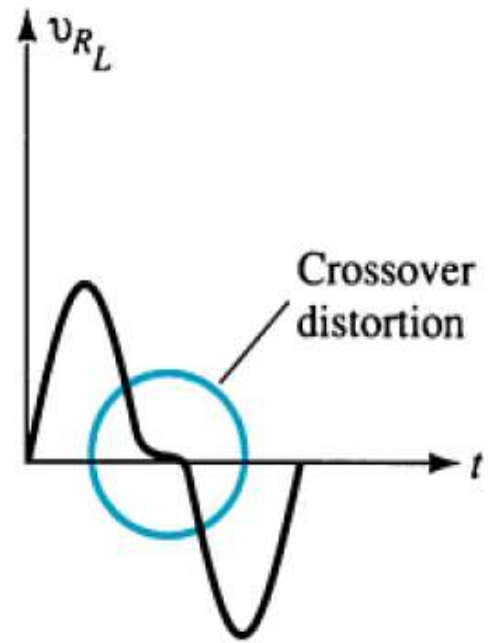
- **During the positive half-cycle of the AC input, transistor Q_1 (*npn*) is conducting and Q_2 (*pnp*) is off.**
- **During the negative half-cycle of the AC input, transistor Q_2 (*pnp*) is conducting and Q_1 (*npn*) is off.**



Each transistor produces one-half of an AC cycle. The transformer combines the two outputs to form a full AC cycle.

Crossover Distortion

If the transistors Q_1 and Q_2 do not turn on and off at exactly the same time, then there is a gap in the output voltage.



Amplifier Distortion

If the output of an amplifier is not a complete AC sine wave, then it is distorting the output. The amplifier is non-linear.

This distortion can be analyzed using Fourier analysis. In Fourier analysis, any distorted periodic waveform can be broken down into frequency components. These components are harmonics of the fundamental frequency.

Harmonics

Harmonics are integer multiples of a fundamental frequency.

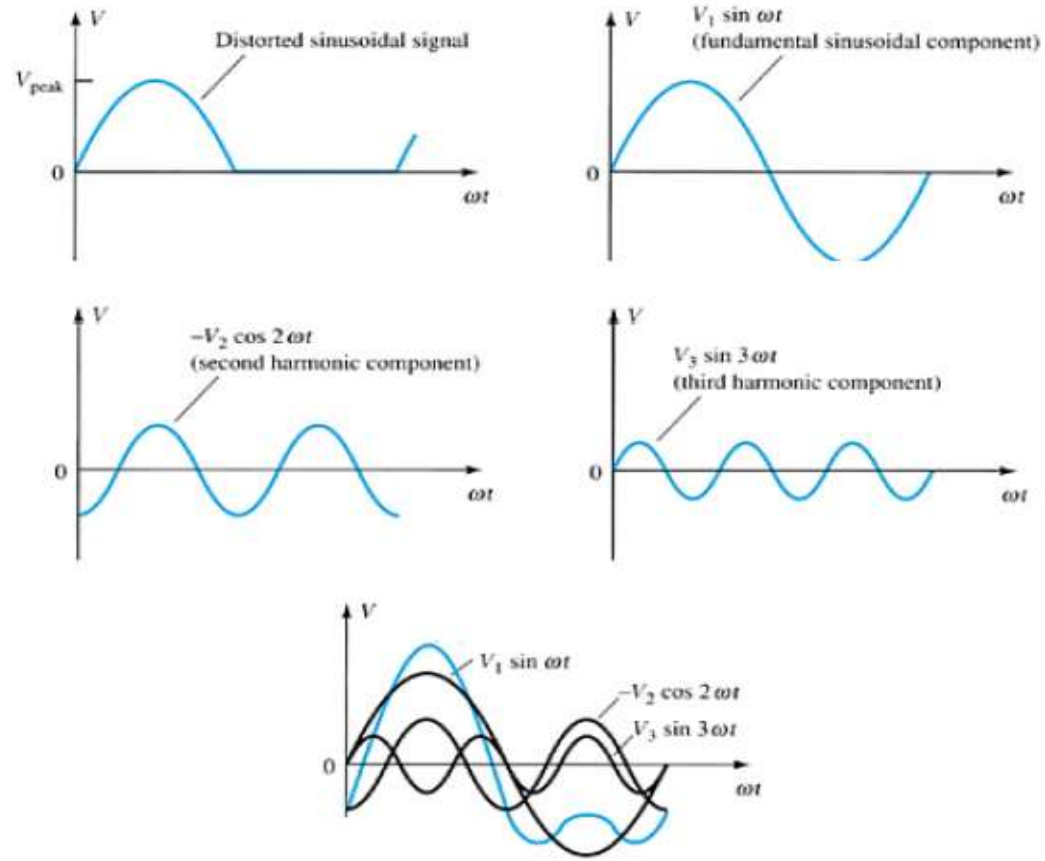
If the fundamental frequency is 5kHz:

1st harmonic	**1 x 5kHz**
2nd harmonic	**2 x 5kHz**
3rd harmonic	**3 x 5kHz**
4th harmonic	**4 x 5kHz**
etc.	

Note that the 1st and 3rd harmonics are called odd harmonics and the 2nd and 4th are called even harmonics.

Harmonic Distortion

According to Fourier analysis, if a signal is not purely sinusoidal, then it contains harmonics.



Harmonic Distortion Calculations

Harmonic distortion (D) can be calculated:

$$\%\ \text{nth harmonic distortion} = \%D_n = \left|\frac{A_n}{A_1}\right| \times 100$$

where

A_n **is the amplitude of the fundamental frequency**

A_n **is the amplitude of the highest harmonic**

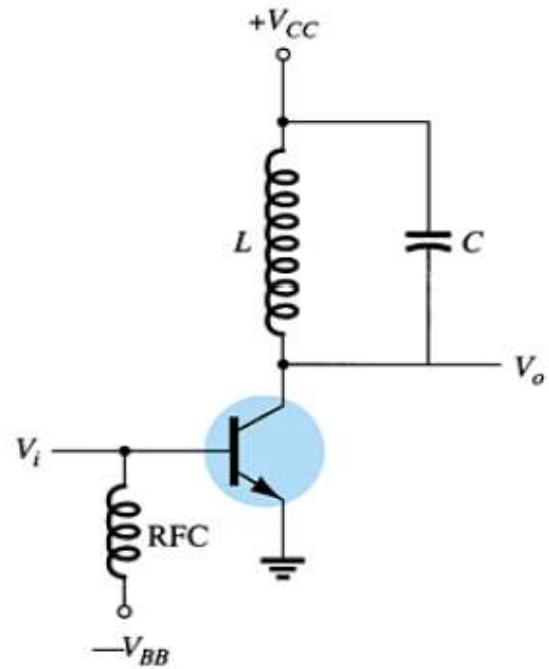
The total harmonic distortion (THD) is determined by:

$$\%\ \text{THD} = \sqrt{D_2^2 + D_3^2 + D_3^2 + \cdots} \times 100$$

Class C Amplifiers

A class C amplifier conducts for less than 180°. In order to produce a full sine wave output, the class C uses a tuned circuit (LC tank) to provide the full AC sine wave.

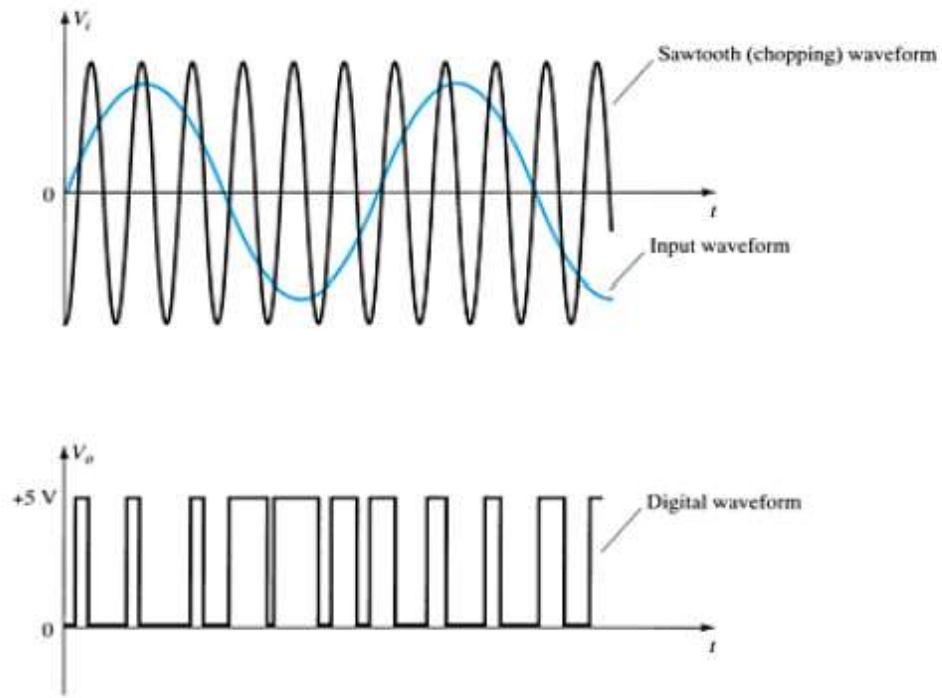
Class C amplifiers are used extensively in radio communications circuits.



Class D Amplifier

A class D amplifier amplifies pulses, and requires a pulsed input.

There are many circuits that can convert a sinusoidal waveform to a pulse, as well as circuits that convert a pulse to a sine wave. This circuit has applications in digital circuitry.

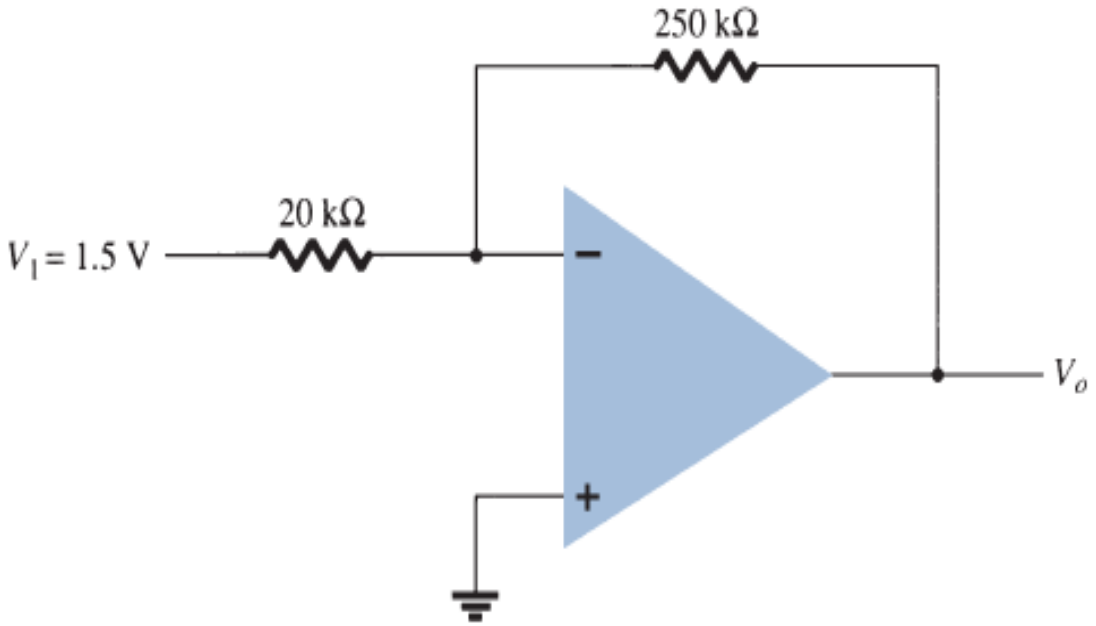


Problems on Op-Amp:

- Ref. Book- R L Boylestd

Problem-1:

What is the output voltage in the circuit

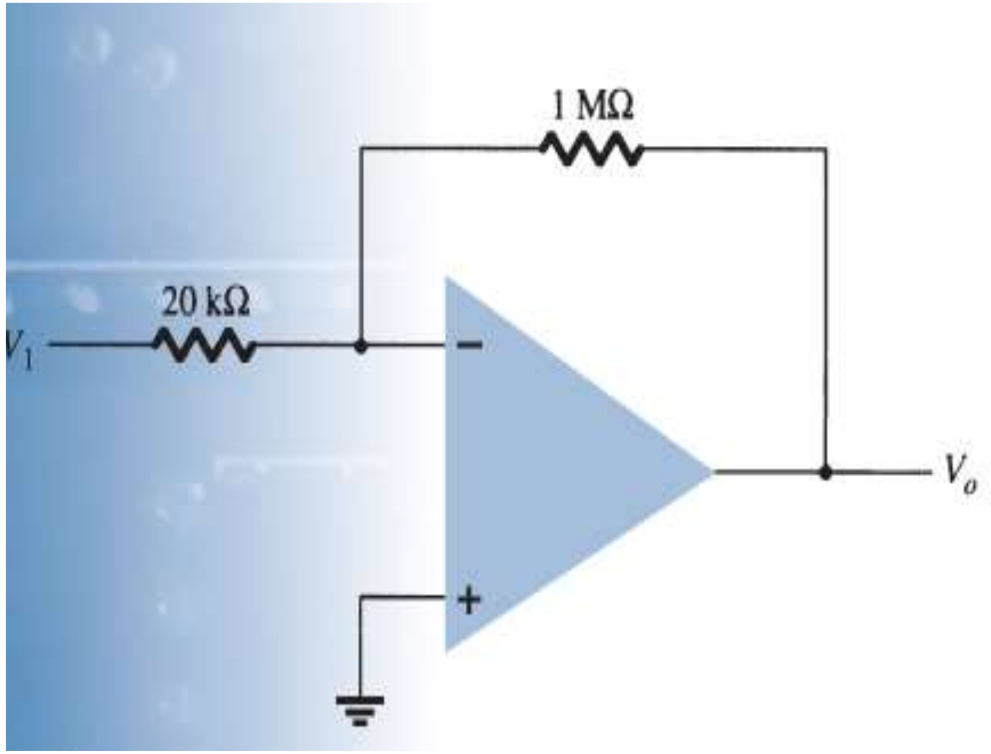


Solution:-1

$$V_o = -\frac{R_F}{R_1}V_1 = -\frac{250\ \text{k}\Omega}{20\ \text{k}\Omega}(1.5\ \text{V}) = \mathbf{-18.75\ V}$$

Problem-2:

What input voltage results in an output of 2 V in the circuit



Solution:-2

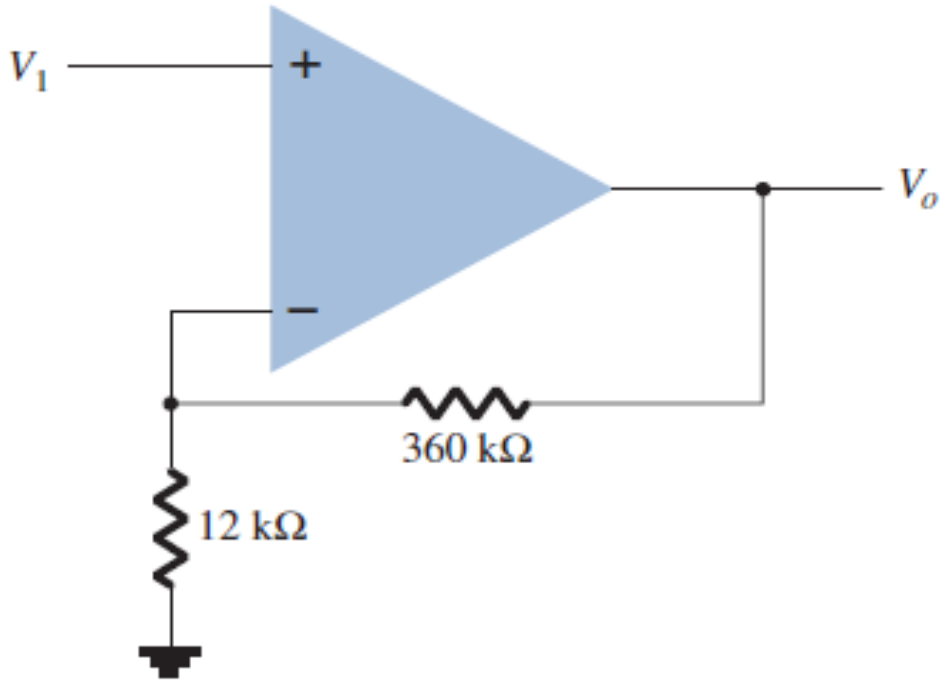
$$V_o = -\frac{R_f}{R_1}V_1 = -\frac{1\ \text{M}\Omega}{20\ \text{k}\Omega}\quad V_1 = 2\ \text{V}$$

$$V_1 = \frac{2\ \text{V}}{-50} = \mathbf{-40\ mV}$$

Problem-3:

1.What output voltage results in the circuit for an input of *V*1=-0.3 V?

2.What input must be applied to the input of Fig to result in an output of 2.4 V?



Solution:-3

$$V_o = \left(1 + \frac{R_F}{R_1}\right) V_1 = \left(1 + \frac{360\ \text{k}\Omega}{12\ \text{k}\Omega}\right) (-0.3\ \text{V})$$

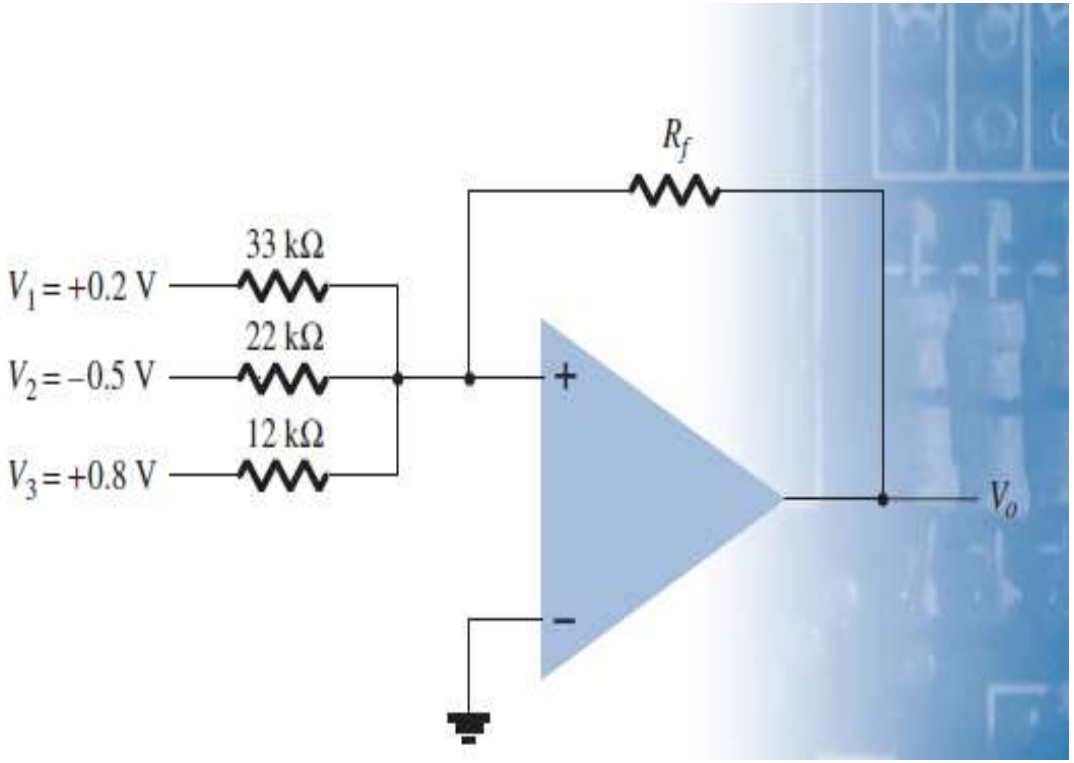
$$= 31(-0.3\ \text{V}) = \mathbf{-9.3\ V}$$

$$V_o = \left(1 + \frac{R_F}{R_1}\right) V_1 = \left(1 + \frac{360\ \text{k}\Omega}{12\ \text{k}\Omega}\right) V_1 = 2.4\ \text{V}$$

$$V_1 = \frac{2.4\ \text{V}}{31} = \mathbf{77.42\ mV}$$

Problem-4:

Calculate the output voltage developed by the circuit of Fig. for $R_f = 330\ \text{k}\Omega$.



Solution:-4

$$V_o = -\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3$$

$$= -\frac{330\ \text{k}\Omega}{33\ \text{k}\Omega}(0.2\ \text{V}) + \frac{330\ \text{k}\Omega}{22\ \text{k}\Omega}(-0.5\ \text{V}) + \frac{330\ \text{k}\Omega}{12\ \text{k}\Omega}(0.8\ \text{V})$$

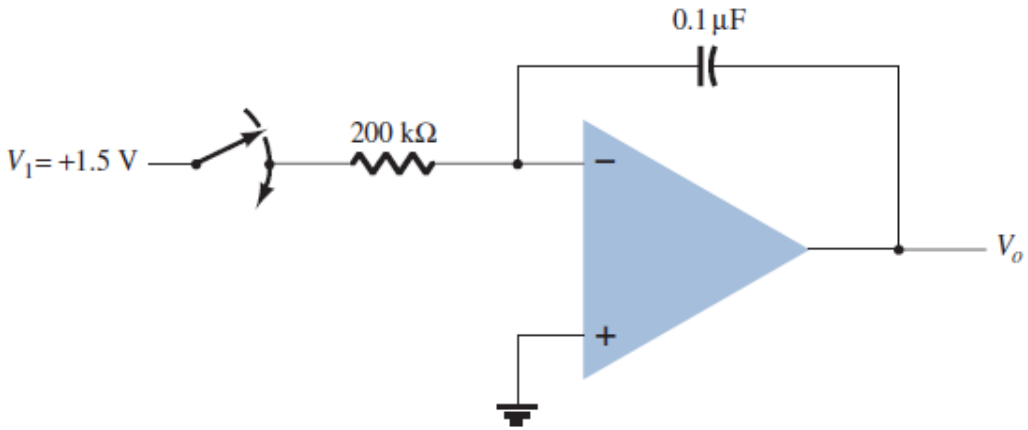
$$= -[10(0.2\ \text{V}) + 15(-0.5\ \text{V}) + 27.5(0.8\ \text{V})]$$

$$= -[2\ \text{V} + (-7.5\ \text{V}) + 2.2\ \text{V}]$$

$$= -[24\ \text{V} - 7.5\ \text{V}] = \mathbf{-16.5\ V}$$

Problem-5:

Find the output waveform

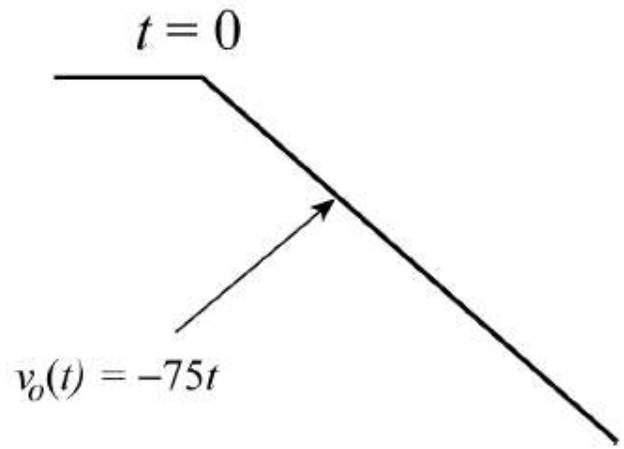


Solution:-5

$$v_o(t) = -\frac{1}{RC} \int v_1(t)\,dt$$

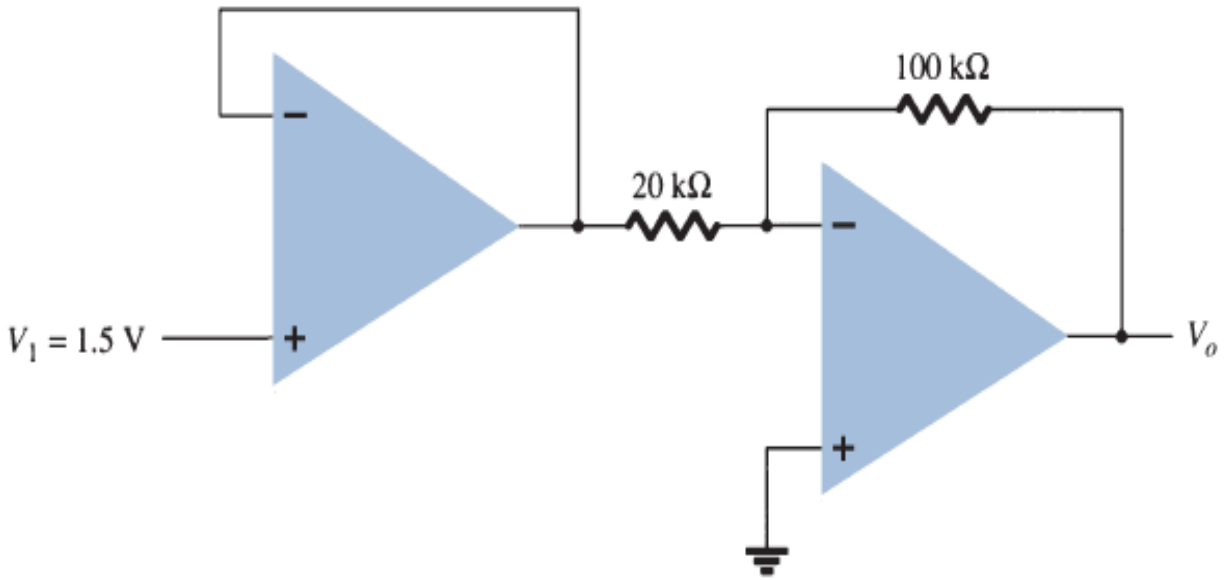
$$= -\frac{1}{(200\ \text{k}\Omega)(0.1\ \mu\text{F})} \int 1.5\,dt$$

$$= -50(1.5t) = \mathbf{-75t}$$



Problem-6:

Calculate the output voltage for the circuit



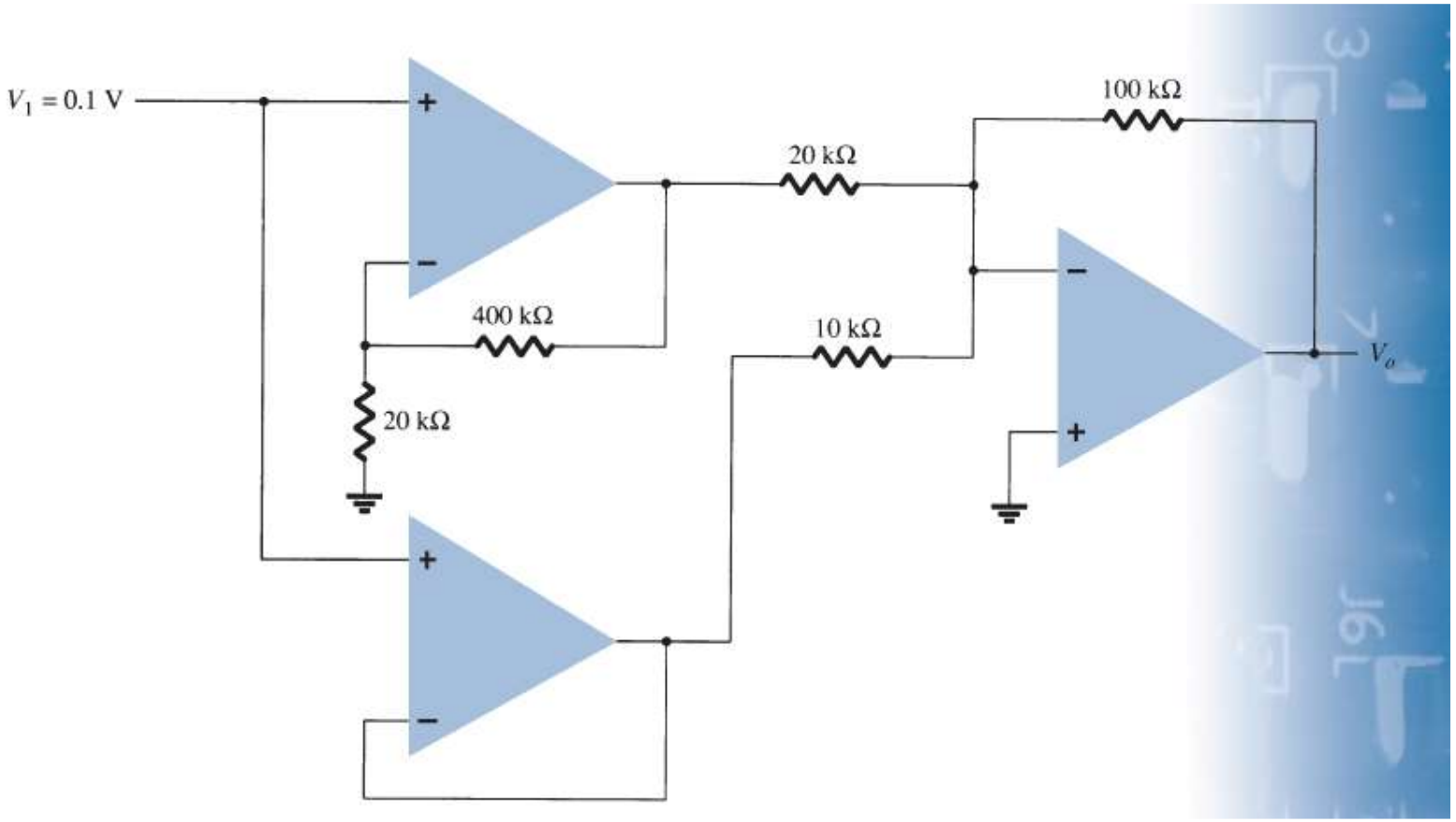
Solution:-6

$$V_o = -\frac{R_f}{R_1}V_1 = -\frac{100\ \text{k}\Omega}{20\ \text{k}\Omega}(1.5\ \text{V})$$

$$= -5(1.5\ \text{V}) = \mathbf{-7.5\ V}$$

Problem-7:

Calculate the output voltage, *Vo*



Solution:-7

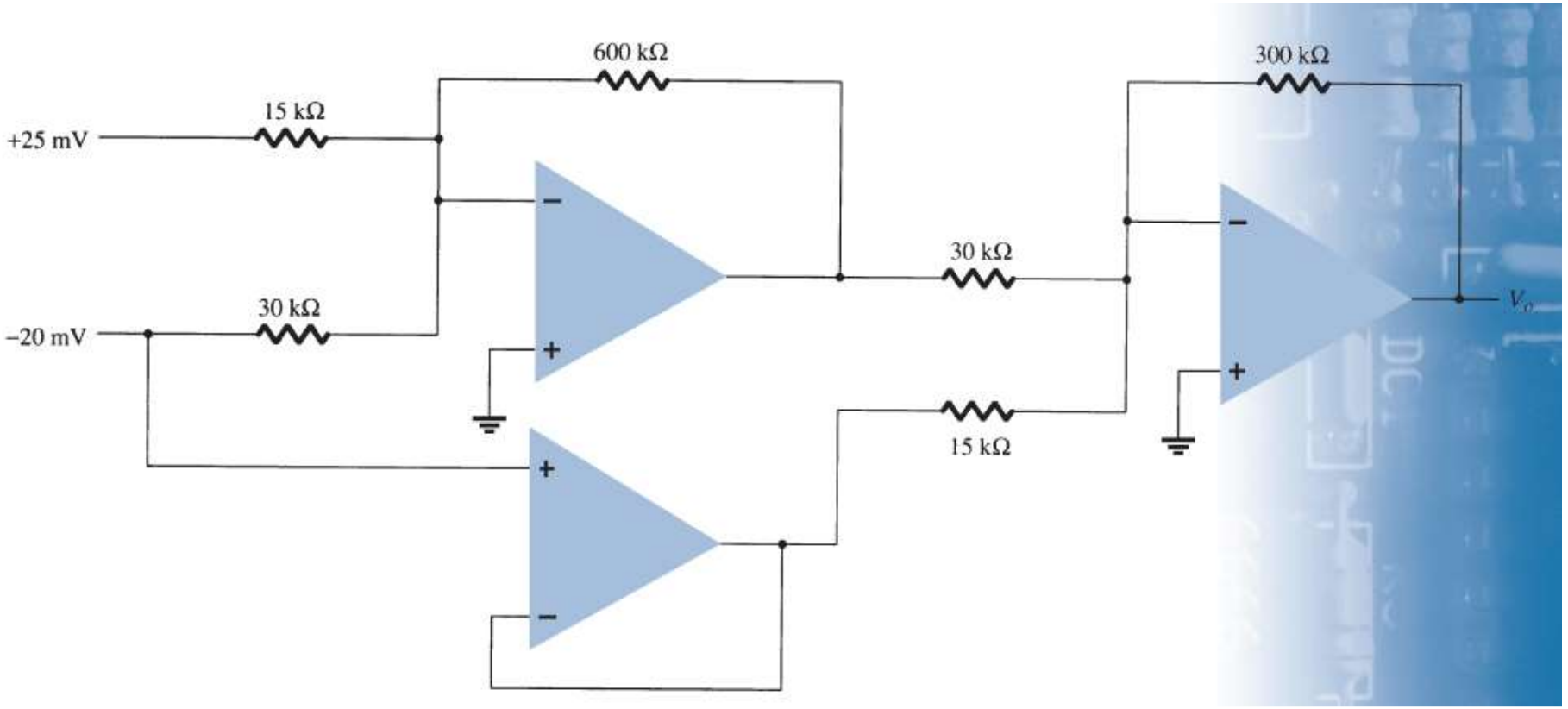
$$V_o = \left(1+\frac{400\ \text{k}\Omega}{20\ \text{k}\Omega}\right)(0.1\ \text{V})\cdot\frac{-100\ \text{k}\Omega}{20\ \text{k}\Omega} + -\frac{100\ \text{k}\Omega}{10\ \text{k}\Omega}(0.1\ \text{V})$$

$$= (2.1\ \text{V})(-5) + (-10)(0.1\ \text{V})$$

$$= -10.5\ \text{V} - 1\ \text{V} = \mathbf{-11.5\ V}$$

Problem-8:

Calculate *Vo* in the circuit



Solution:-8

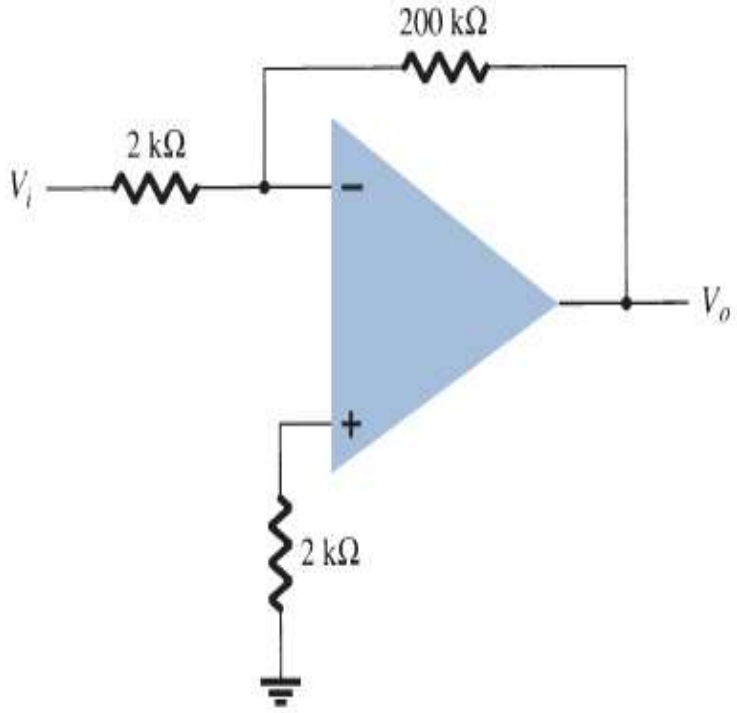
$$V_o = -\frac{600\ \text{k}\Omega}{15\ \text{k}\Omega}(25\ \text{mV}) + \frac{600\ \text{k}\Omega}{30\ \text{k}\Omega}(-20\ \text{mV}) - \frac{300\ \text{k}\Omega}{30\ \text{k}\Omega}$$

$$+ - \frac{300\ \text{k}\Omega}{15\ \text{k}\Omega}(-20\ \text{mV})$$

$$= -[40(25\ \text{mV}) + (20)(-20\ \text{mV})](-10) + (-20)(-20\ \text{mV})$$
$$= -[1\ \text{V} - 0.4\ \text{V}](-10) + 0.4\ \text{V}$$
$$= 6\ \text{V} + 0.4\ \text{V} = \mathbf{6.4\ V}$$

Problem-9:

Calculate the total offset voltage for the circuit of Fig. for an op-amp with specified values of
input offset voltage V_{IO} = 6 mV and input offset current I_{IO} = 120 nA.



Solution:-9

$$V_o = \left(1 + \frac{R_f}{R_1}\right) V_{Io} + I_{Io} R_f$$

$$= \left(1 + \frac{200\ \text{k}\Omega}{2\ \text{k}\Omega}\right) (6\ \text{mV}) + (120\ \text{nA})(200\ \text{k}\Omega)$$

$$= 101(6\ \text{mV}) + 24\ \text{mV}$$

$$= 606\ \text{mV} + 24\ \text{mV} = \mathbf{630\ mV}$$

Problem-10

Determine the cutoff frequency of an op-amp having specified values $B_1 = 800$ kHz and $A_{VD} = 150$ V/mV.

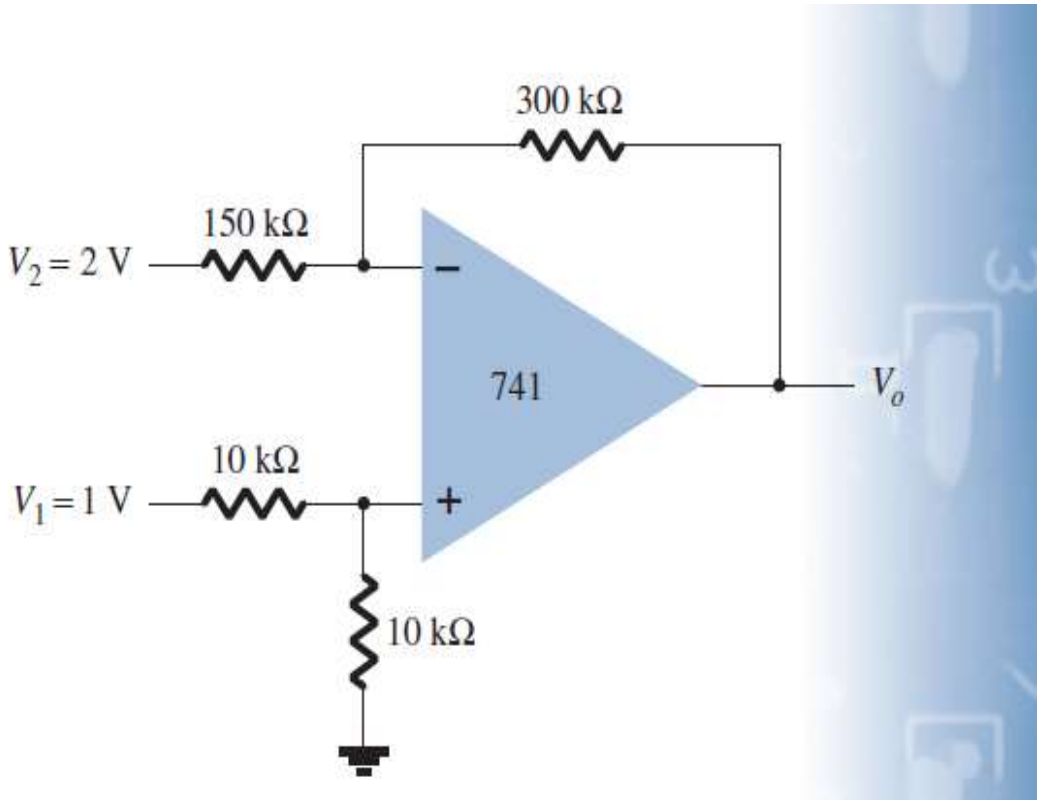
Solution:-10

$$f_1 = 800 \text{ kHz}$$

$$f_c = \frac{f_1}{A_{v_2}} = \frac{800 \text{ kHz}}{150 \times 10^3} = 5.3 \text{ Hz}$$

Problem-11

Determine the output voltage for the circuit

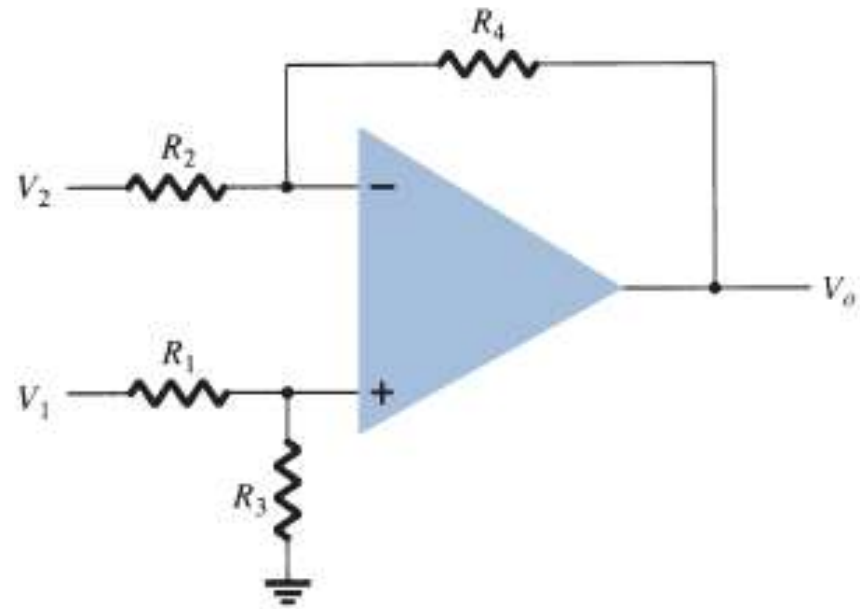


Solution:-11

$$V_o = \frac{R_3}{R_1 + R_3}\frac{R_2 + R_4}{R_2}V_1 - \frac{R_4}{R_2}V_2$$

$$V_o = \frac{10\ \text{k}\Omega}{10\ \text{k}\Omega + 10\ \text{k}\Omega}\ \frac{150\ \text{k}\Omega + 300\ \text{k}\Omega}{150\ \text{k}\Omega}\ V_1 - \frac{300\ \text{k}\Omega}{150\ \text{k}\Omega}V_2$$

$$= 0.5(3)(1\ \text{V}) - 2(2\ \text{V}) = 1.5\ \text{V} - 4\ \text{V} = \mathbf{-2.5\ V}$$



Subtraction circuit.

Problem-12

Calculate the CMRR (in dB) for the circuit measurements of $V_d = 1\,\text{mV}$, $V_o = 120\,\text{mV}$, $V_C = 1\,\text{mV}$, and $V_o = 20\,\mu\text{V}$.

Solution:-12

$$A_d = \frac{V_o}{V_d} = \frac{120\ \text{mV}}{1\ \text{mV}} = 120$$

$$A_c = \frac{V_o}{V_c} = \frac{20\ \mu\text{V}}{1\ \text{mV}} = 20 \times 10^{-3}$$

$$\text{Gain (dB)} = 20 \log \frac{A_d}{A_c} = 20 \log \frac{120}{20 \times 10^{-3}}$$

$$= 20 \log(6 \times 10^3) = \mathbf{75.56\ dB}$$

Problem-13

For an op-amp having a slew rate of SR $= 2.4\ \text{V}/\mu\text{s}$, what is the maximum closed-loop voltage gain that can be used when the input signal varies by 0.3 V in 10 μs?

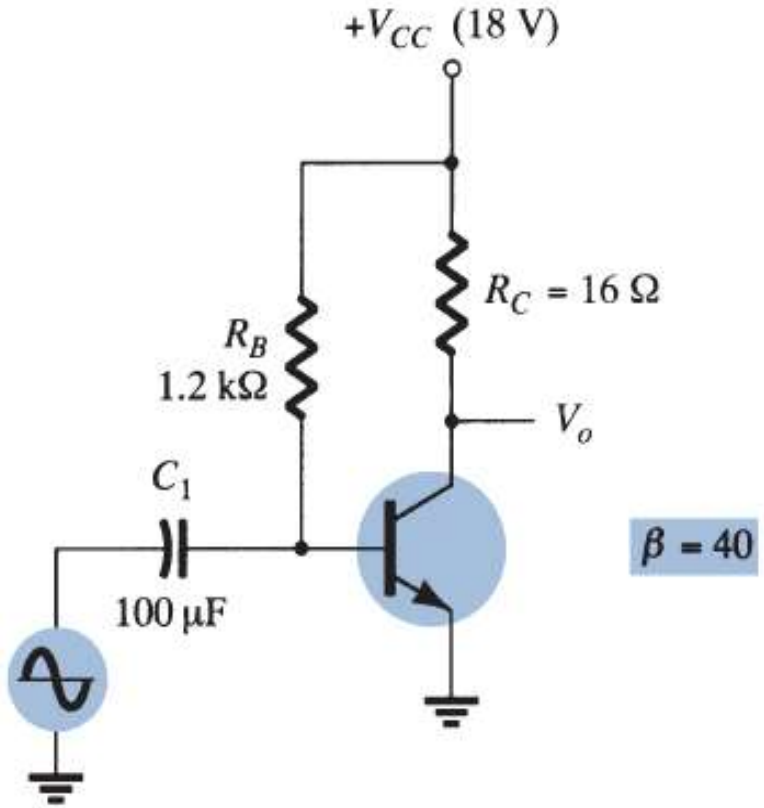
Solution:-13

$$A_{CL} = \frac{SR}{\Delta V_i / \Delta t} = \frac{2.4\ \text{V}/\mu s}{0.3\ \text{V}/10\ \mu s} = \mathbf{80}$$

Problem-14

Calculate the input and output power for the circuit of Fig.

The input signal results in a base current of 5 mA rms.



Solution:-14

$$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{18\text{ V} - 0.7\text{ V}}{1.2\text{ k}\Omega} = 14.42\text{ mA}$$

$$I_{C_Q} = \beta I_{B_Q} = 40(14.42\text{ mA}) = 576.67\text{ mA}$$

$$P_i = V_{CC} I_{dc} \cong V_{CC} I_{C_Q} = (18\text{ V})(576.67\text{ mA})$$

$$\cong \mathbf{10.4\text{ W}}$$

$$I_C(\text{rms}) = \beta I_B(\text{rms})$$

$$= 40(5\text{ mA}) = 200\text{ mA}$$

$$P_o = I_C^2(\text{rms}) R_C = (200\text{ mA})^2(16\ \Omega) = \mathbf{640\text{ mW}}$$