END SEMESTER EXAMINATION

COURSE NAME: **B. Tech** SEMESTER: **3rd**

BRANCH NAME: **Computer Science & Engineering / Information Technology**

SUBJECT NAME: **Digital Logic Design**

FULL MARKS: **50** TIME: **2.5** Hours

Answer **All** Questions.

The figures in the right-hand margin indicate Marks. *Symbols carry usual meaning.*

Q1. Answer all Questions. **[2×5]**

a) Convert 937.25 to equivalent BCD and Excess-3 code.

b) What is Gate delay? Is it different from Propagation delay? Justify your answer.

c) Whether Decoder can be used as a Demultiplexer? Justify your answer.

d) What do you mean by the edge triggering and level triggering? Explain with diagram.

e) How many Flip Flops are required for MOD-12 Ring counter and Twisted ring counter respectively?

Q2.

a) What will be the range of n-bit binary number if that will be represented as Signed magnitude representation, Signed 1's complement representation and Signed 2's complement representation **[6]**

b) Whether Gray code is a reflected code? Justify your answer. **[2]**

OR

a) Find out the result of the following subtraction operations using 2's Complement method, if X = 1011100 and Y = 1011011. **[6]**

(i) X - Y *(ii)* Y - X

b) Whether Excess-3 code is self-complementary? Justify your answer. **[2]**

Q3.

a) Simplify the Boolean equation $f(w, x, y, z) = \Sigma m(0, 2, 4, 6, 8) + \Sigma d(10, 11, 12, 13, 14, 15)$ and realize it using NAND gates only. **[6]**

b) Explain the Absorption law with example. **[2]**

OR

a) Simplify the Boolean equation $F = A'B'D' + A'CD + A'BC'$, $d = A'BC'D + ACD + AB'D'$ and realize it using NOR gates only. **[6]**

b) Realize an EX-OR gate using minimum numbers of NAND gates? **[2]**

Q4.

a) What is Priority Encoder? State the Truth Table and design a 4-to-2 Priority Encoder. **[5]**

b) Design and explain an Error detection circuit using Odd parity generator and checker. **[3]**

OR

a) F = x' y z + x y' z' + x y' z + x y z' **[5]**

Implement the above expression using 4-to-1 Multiplexer.

b) Implement Full Subtractor circuit using Decoder. [3]

Q5.

a) What is Race around condition? How Race around condition can be avoided by using Master Slave JK flip flop? Explain with proper diagram. [5]

b) Distinguish and differentiate between Characteristic Table and Excitation Table with example. [3]

OR

a) What is Universal Shift Register? Describe the operation of a 3-bit Universal Shift Register with proper logic diagram. [5]

b) What is Setup time and Hold time? Explain with proper timing diagram. [3]

Q6.

a) What is Decade counter? Design a Synchronous decade counter using JK flip-flop. [5]

b) What is Ring counter? Design and explain a 4-bit Ring counter with timing diagram. [3]

OR

a) What do you mean by Modulus of a counter? Design a Synchronous counter using D-flip flop to generate the count sequence 0, 3, 2, 6, 5, 1, and repeat. [5]

b) Distinguish and differentiate between Synchronous Counter and Asynchronous Counter. [3]