VEER SURENDRA SAI UNIVERSITY OF TECHNOLOGY (VSSUT), ODISHA

Odd Mid Semester Examination for Academic Session 2024-25

COURSE NAME: B. Tech SEMESTER:3rd

BRANCH NAME: Computer Science & Engineering / Information Technology

SUBJECT NAME: Digital Logic Design

FULL MARKS:30 TIME:90 Minutes

Answer AllQuestions.

The figures in the right hand margin indicate Marks. *Symbols carry usual meaning.*

Q1. Answer all Questions. [2×3]

a) Step by step solve the followings. - CO1

$(3B7D)_{16} = (?)_2$ $(31.46)_8 = (?)_{10}$

b) Which Gate is called as Equivalence Gate and why? Justify. - CO2

c) For a data, Hamming code 1010111 is received. What will be the correct data assuming Odd parity checker? - CO3

Q2 [8]

a) Convert $(11010010)_2$ to Gray code and Excess-3 code. - CO1

b) Whether Excess-3 code is a self-complementary code? Justify your answer. -CO1

OR

a) Perform the following operations using 2's complement method. - CO1

11011 – 10011 10010 – 00111

b) Distinguish and differentiate between Combinational circuit and Sequential circuit with example. -CO1

Q3 [8]

Differentiate between Canonical form and Standard form of a Boolean expression and simplify the following Boolean expressions. - CO2

i. F(A, B, C, D) = AB'C' + ABC' + B'C'D + ACD +A' C'

ii. F(A, B, C, D) = (A'+B+C)(B+C+D')(A+C'+D')

OR

a) Simplify the expression F= Π M (1, 3, 5, 12, 13, 14, 15) + d (2, 4, 7, 10). Implement it using universal logic gate. - CO2

b) Simplify the expression F=∑ m (1, 2, 5, 6, 8, 10, 11, 12, 14, 15). Implement it using logic gates. -CO2

Q4 [8]

Step by step derive design logic and design a BCD Subtractor circuit for subtraction of two 4-bit BCD number. Explain with example. - CO3

OR

a) Implement the following Boolean function using multiplexer. - CO3

F(A, B, C, D) = ∑m(1,3,5,6,7,10,13,14,15)

b) Design 1to 8 Demultiplexer using 1 to 4 Demultiplexer and explain the functionality. - CO3